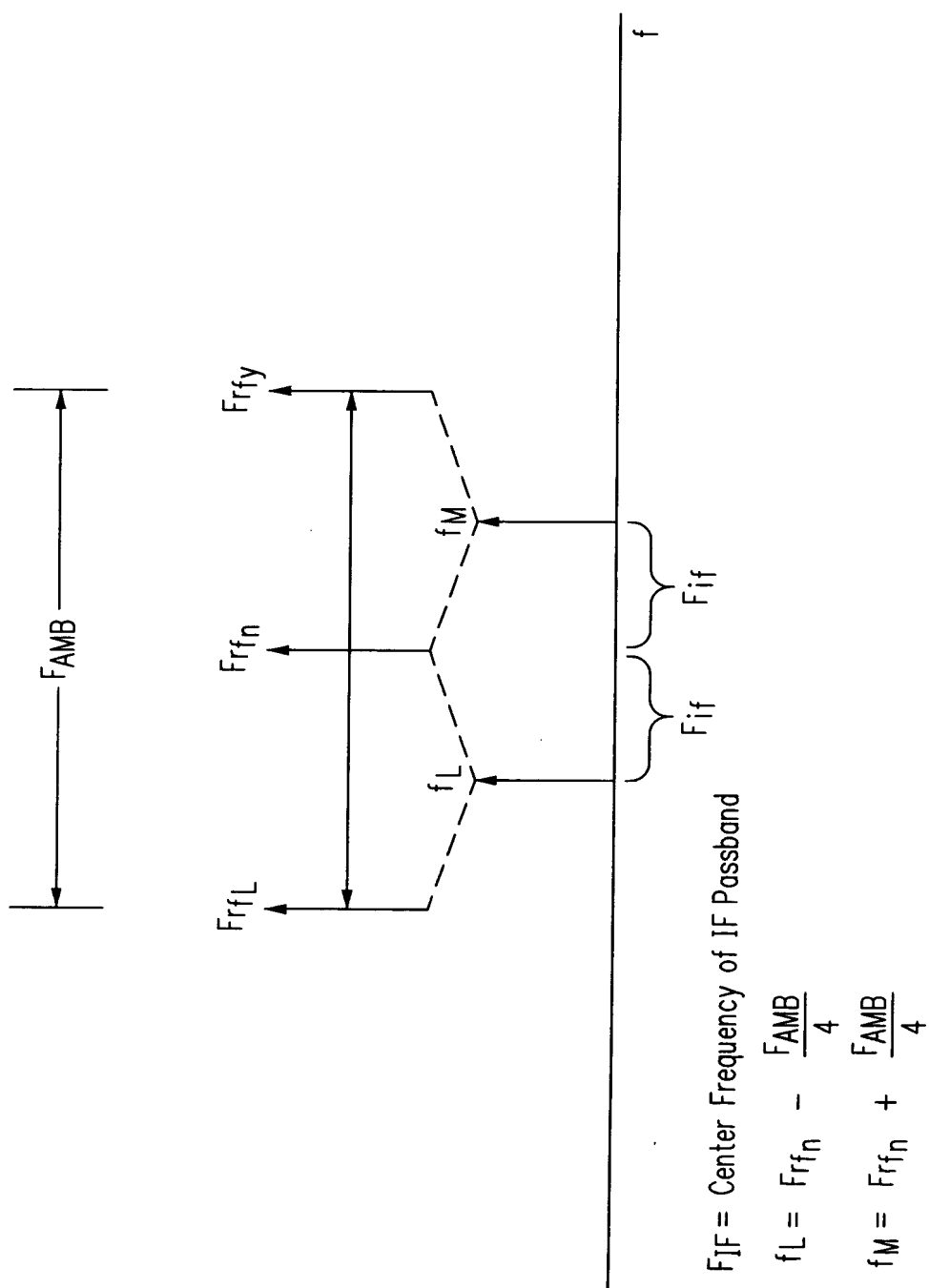


FIG. 1 FULLY INTEGRATED CMOS AM RECEIVER



OPTIMUM LO SWEEP RANGE

FIG. 3

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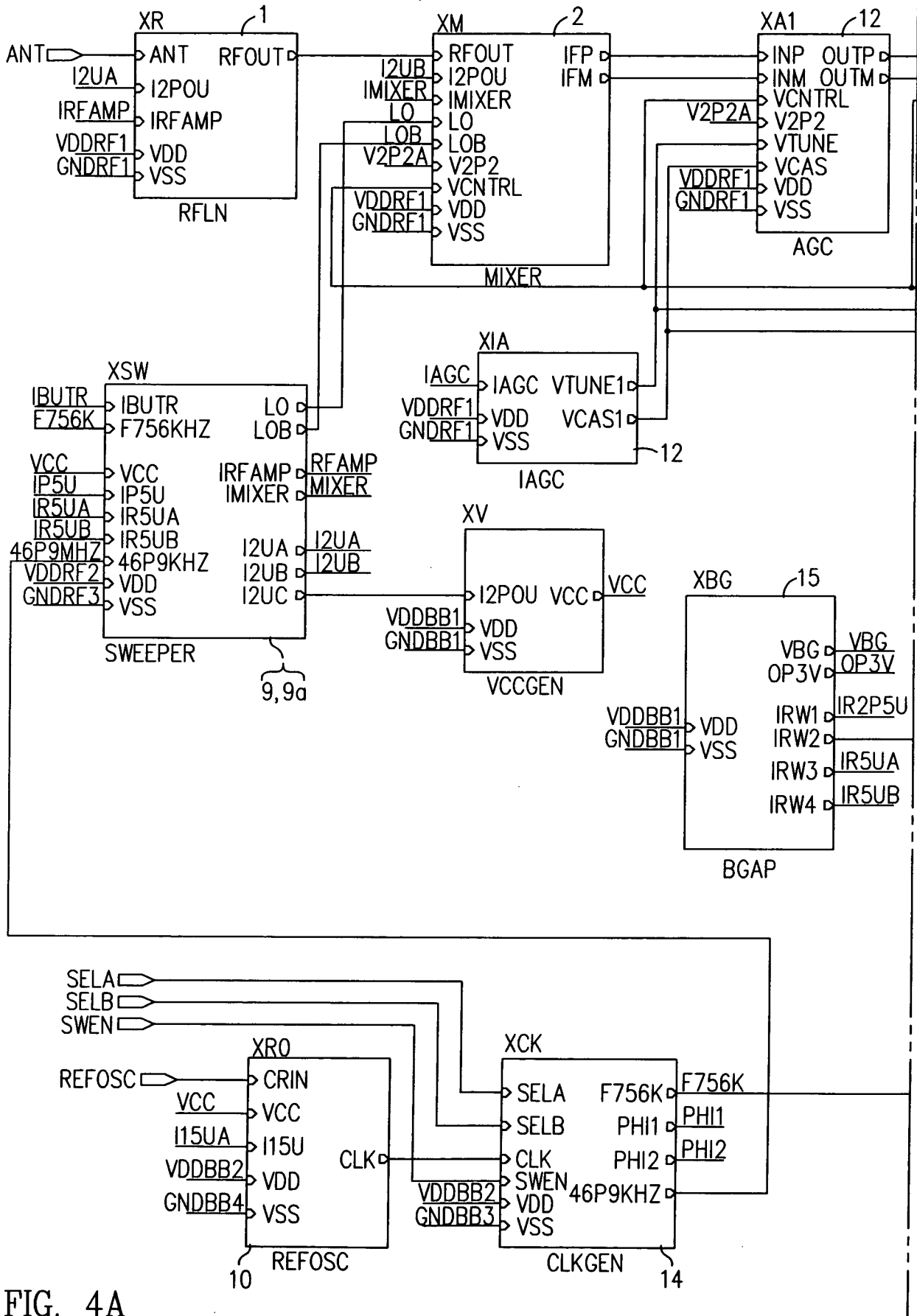


FIG. 4A

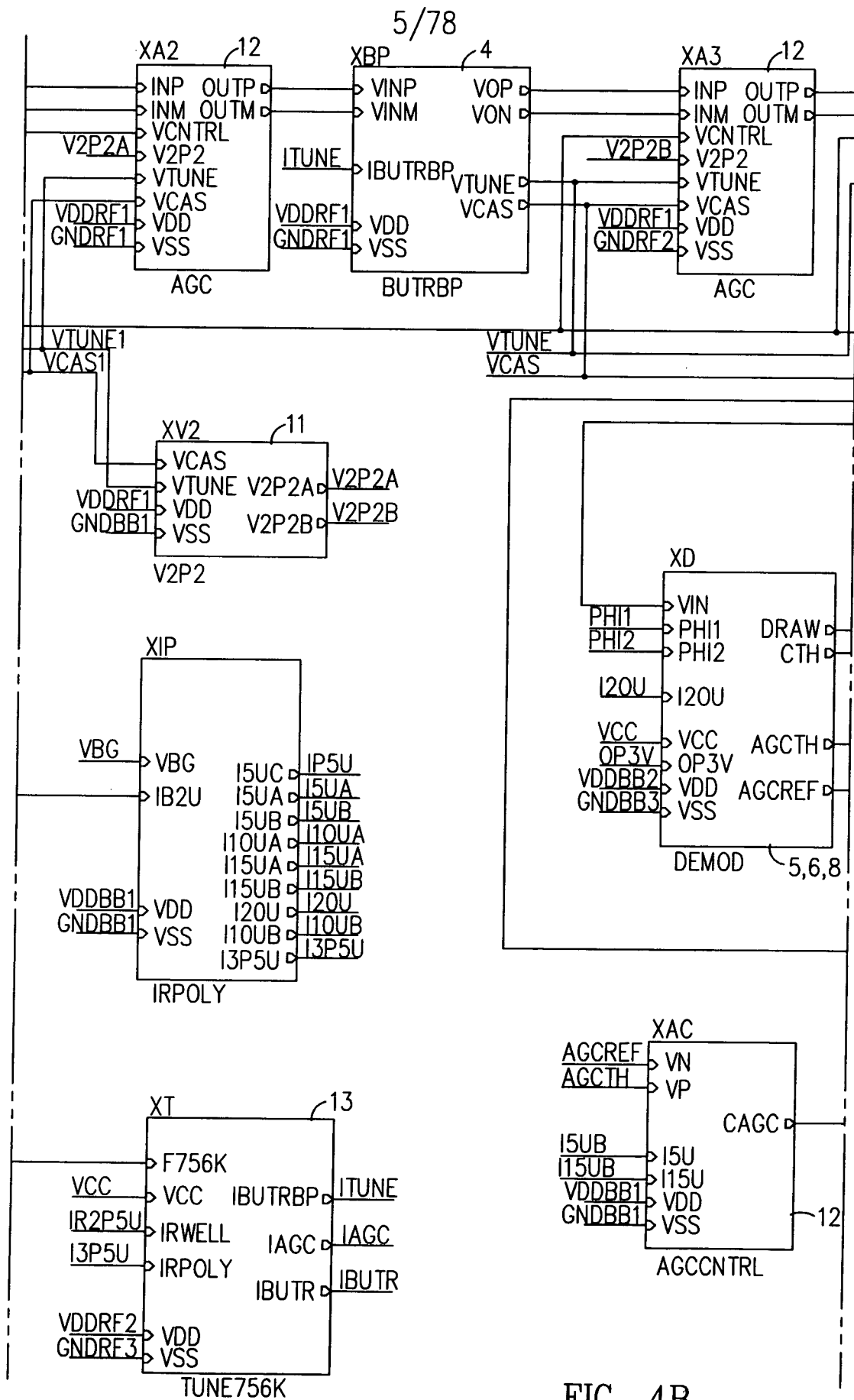


FIG. 4B

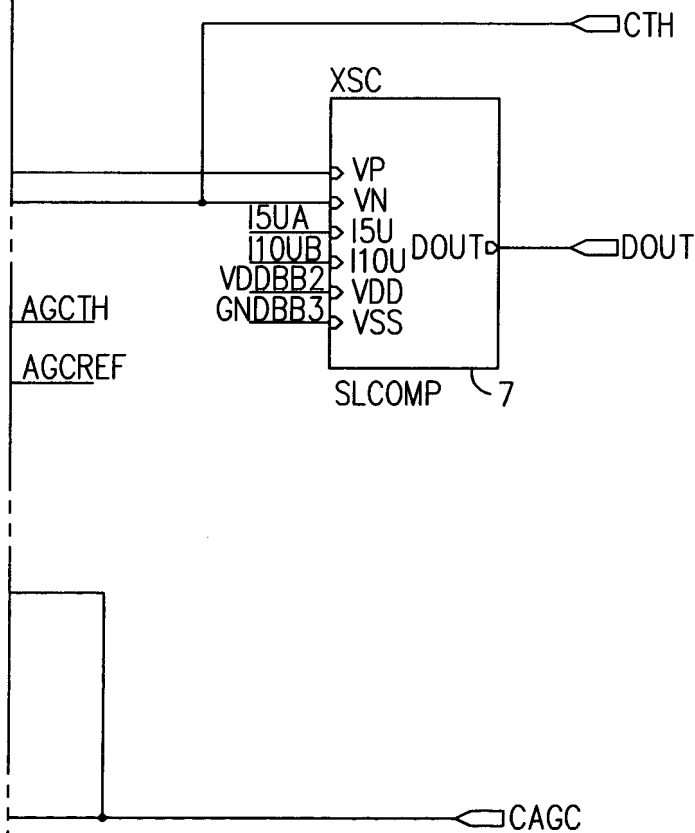
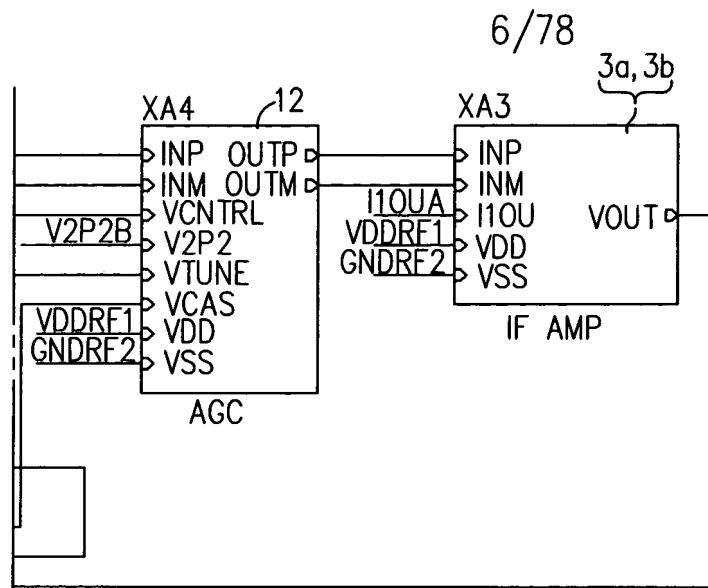
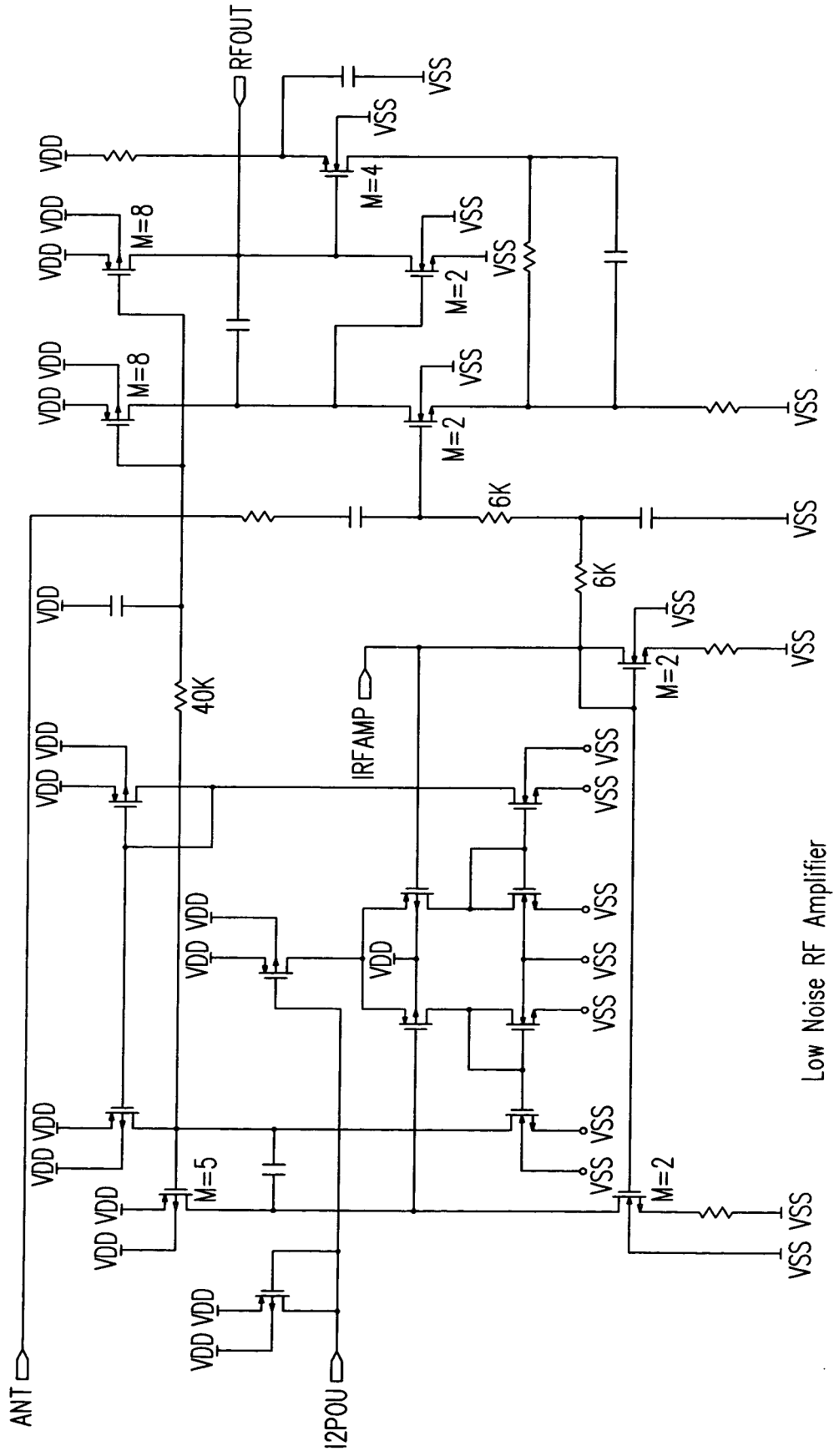


FIG. 4A	FIG. 4B	FIG. 4C
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KEY TO FIG. 4

FIG. 4C



Low Noise RF Amplifier

FIG. 5

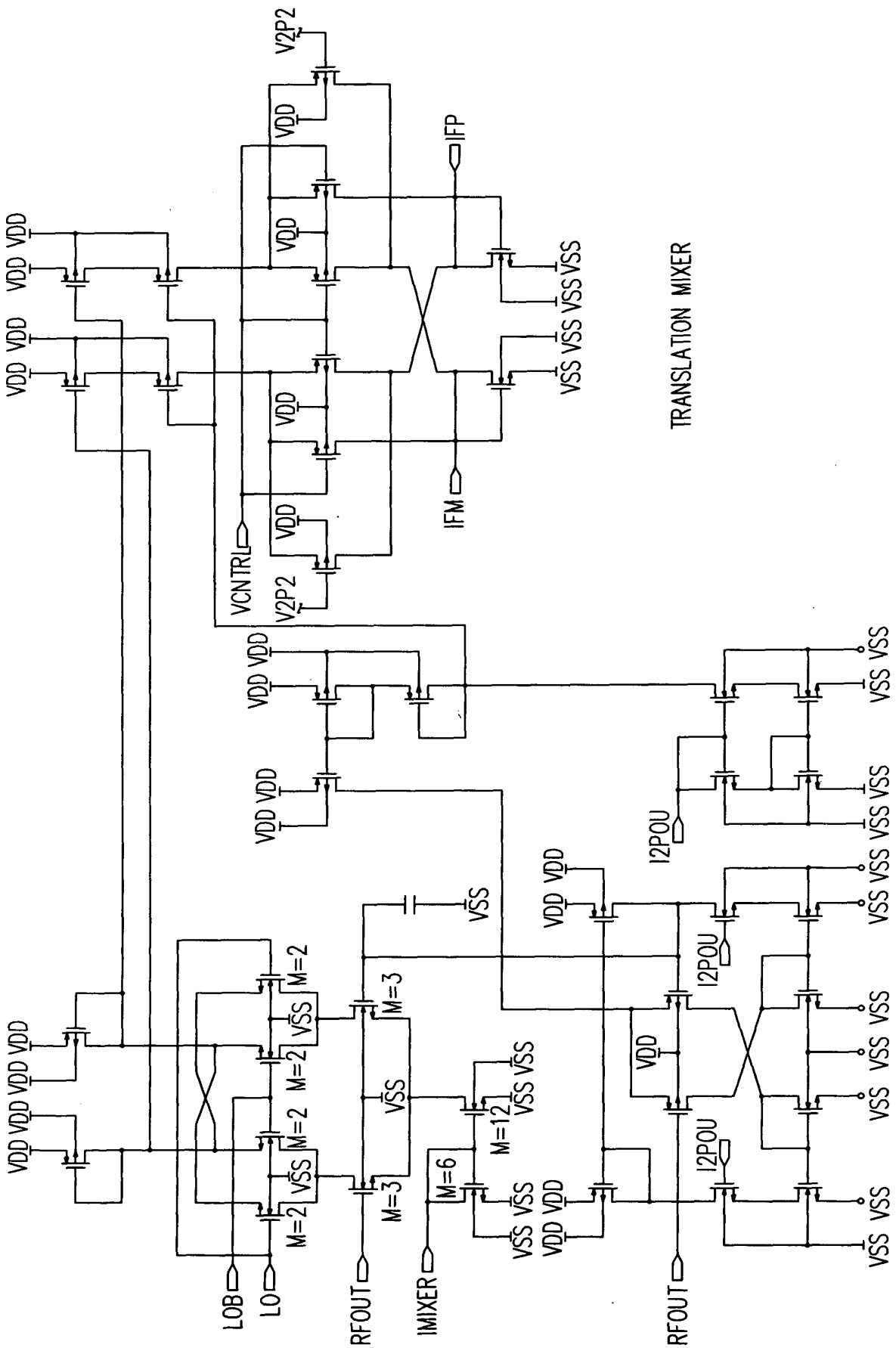


FIG. 6

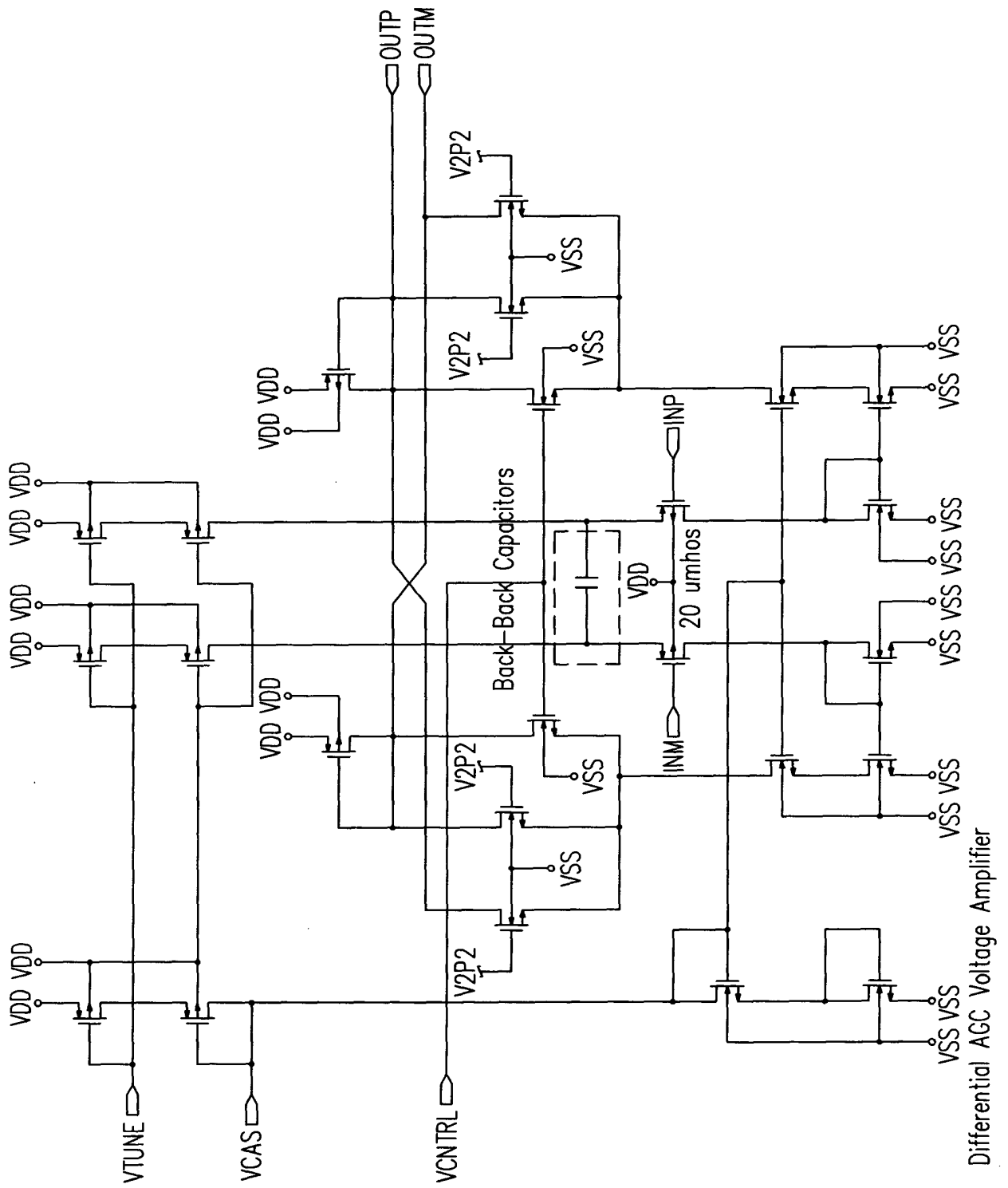
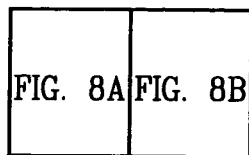


FIG. 7

Differential AGC Voltage Amplifier



KEY TO FIG. 8

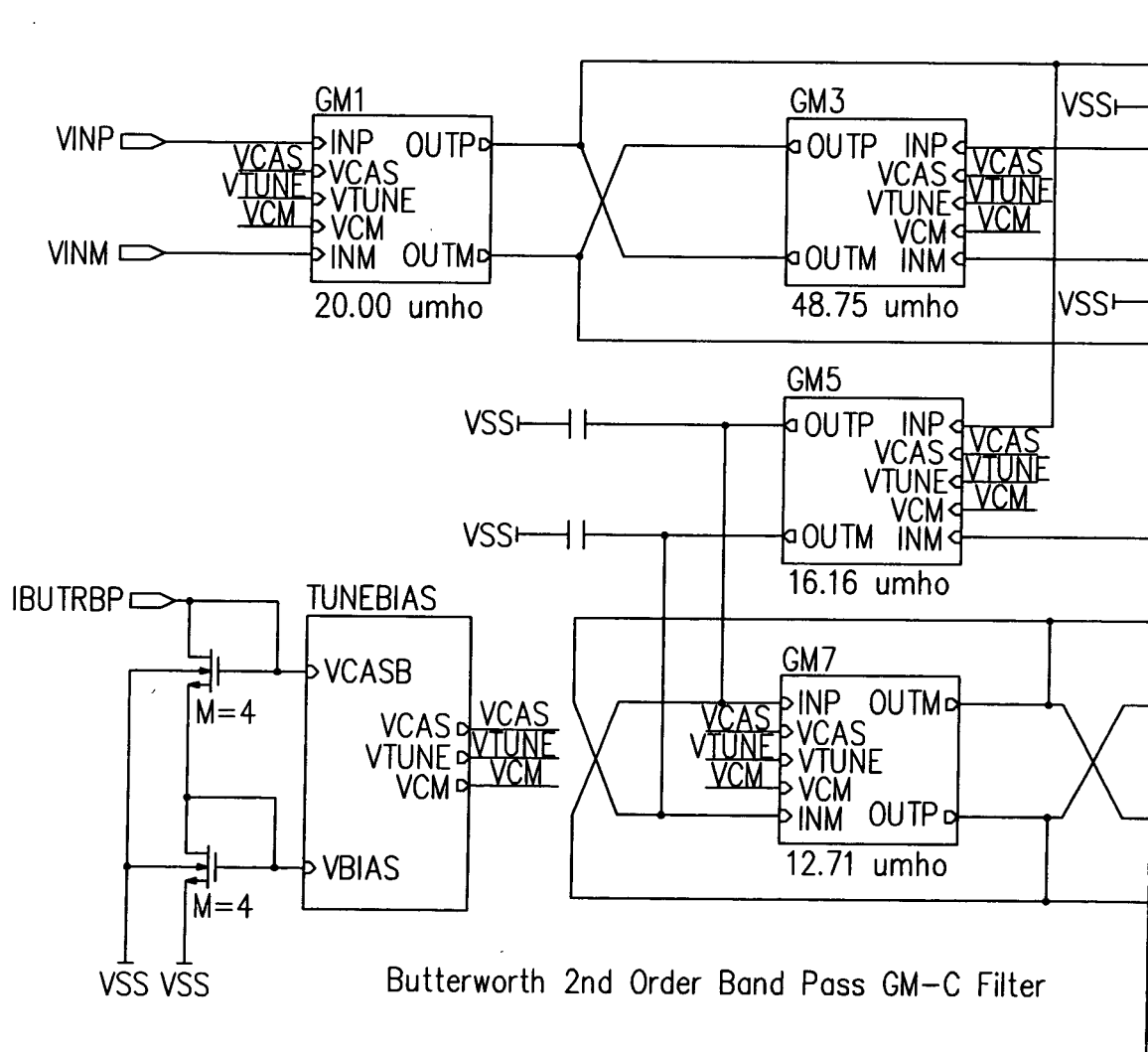


FIG. 8A

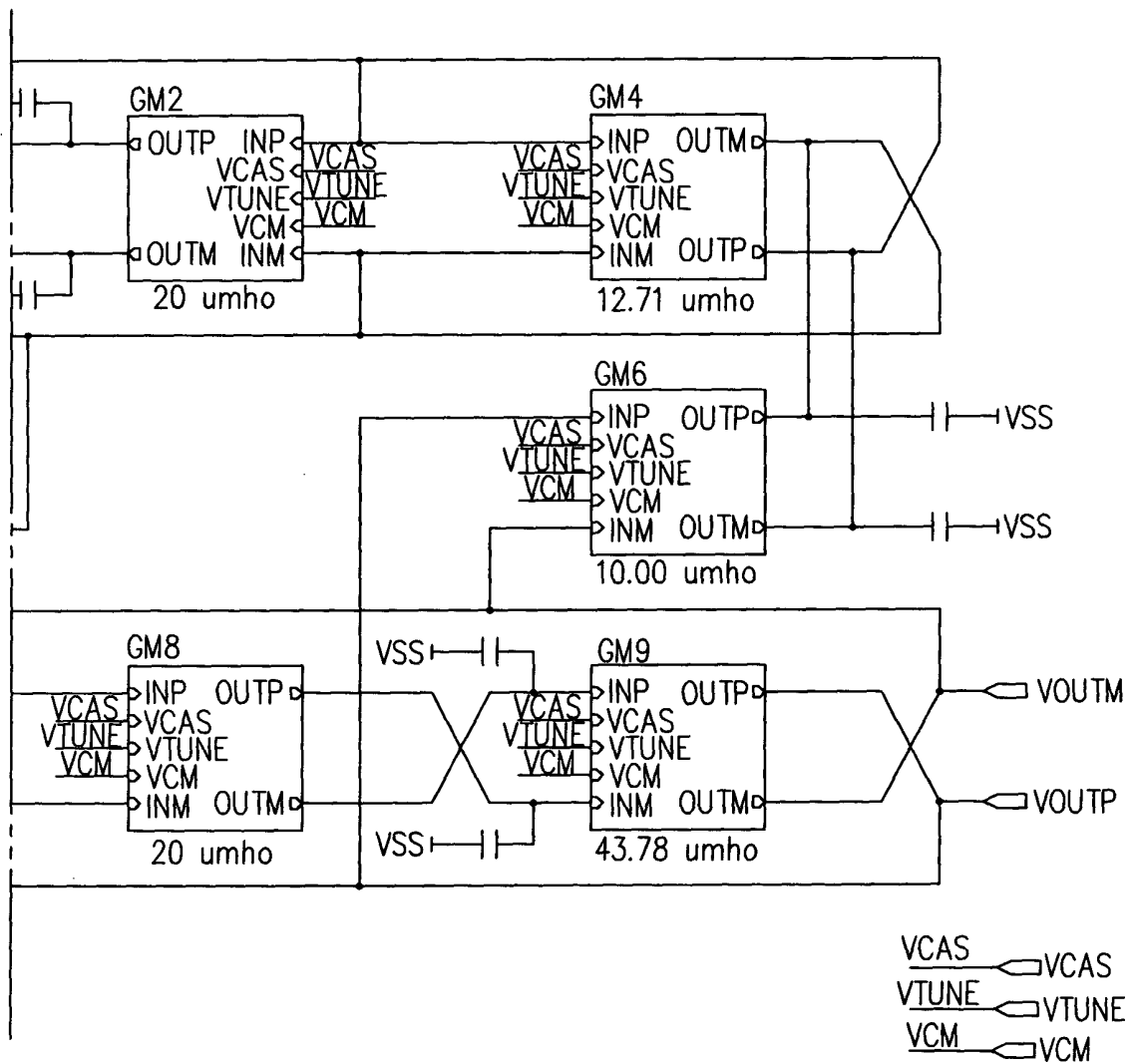


FIG. 8B

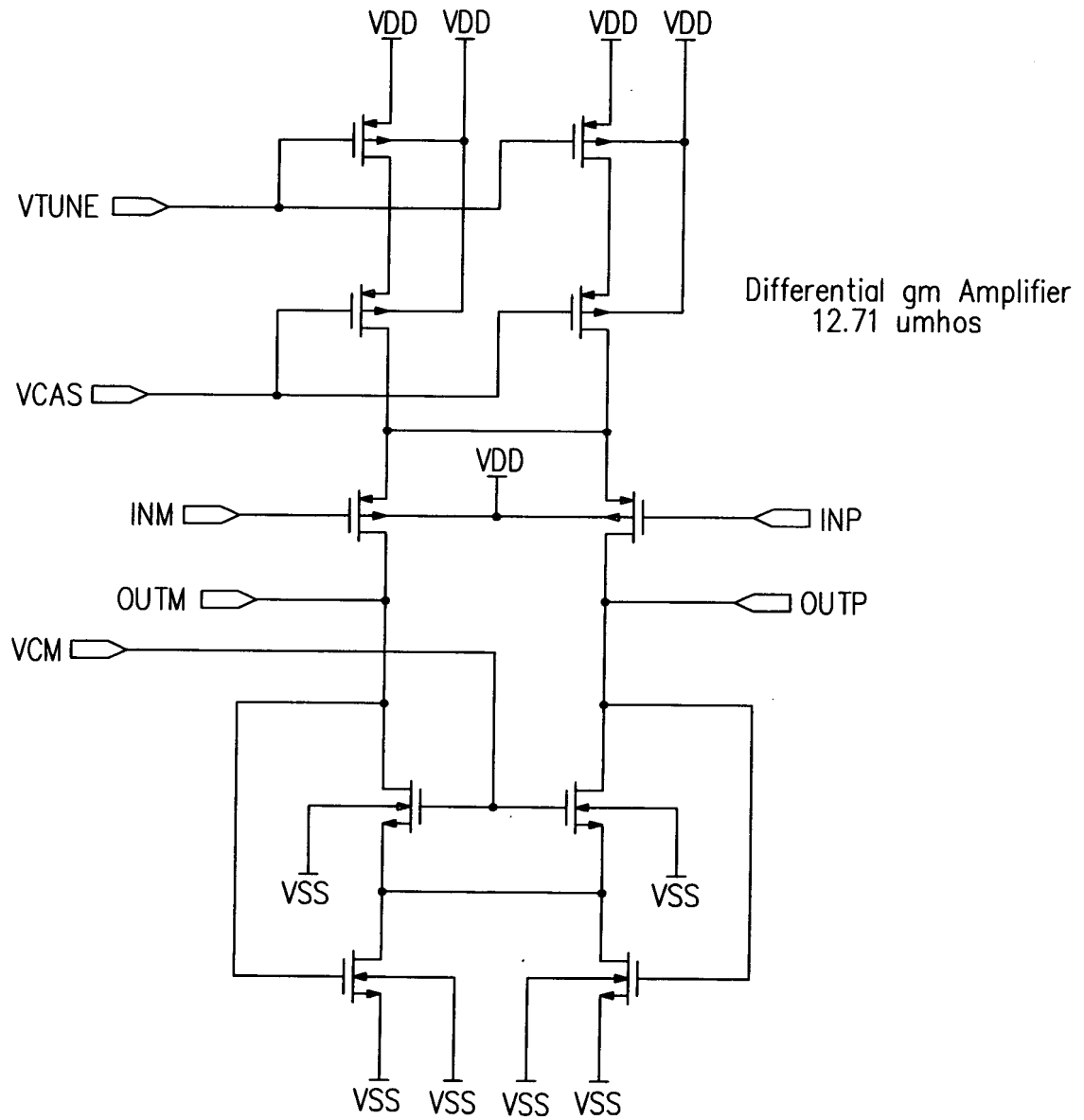


FIG. 9

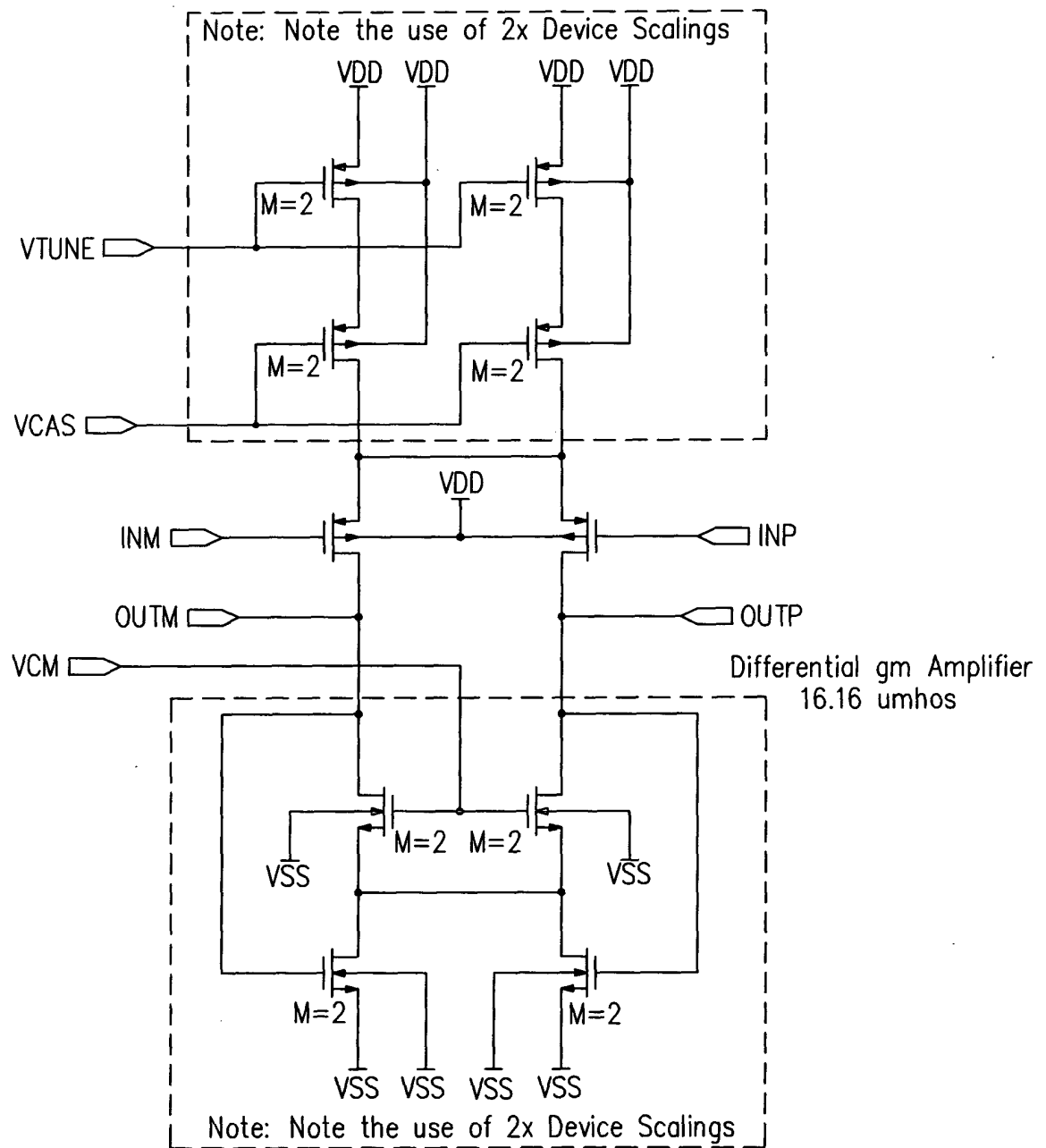


FIG. 10

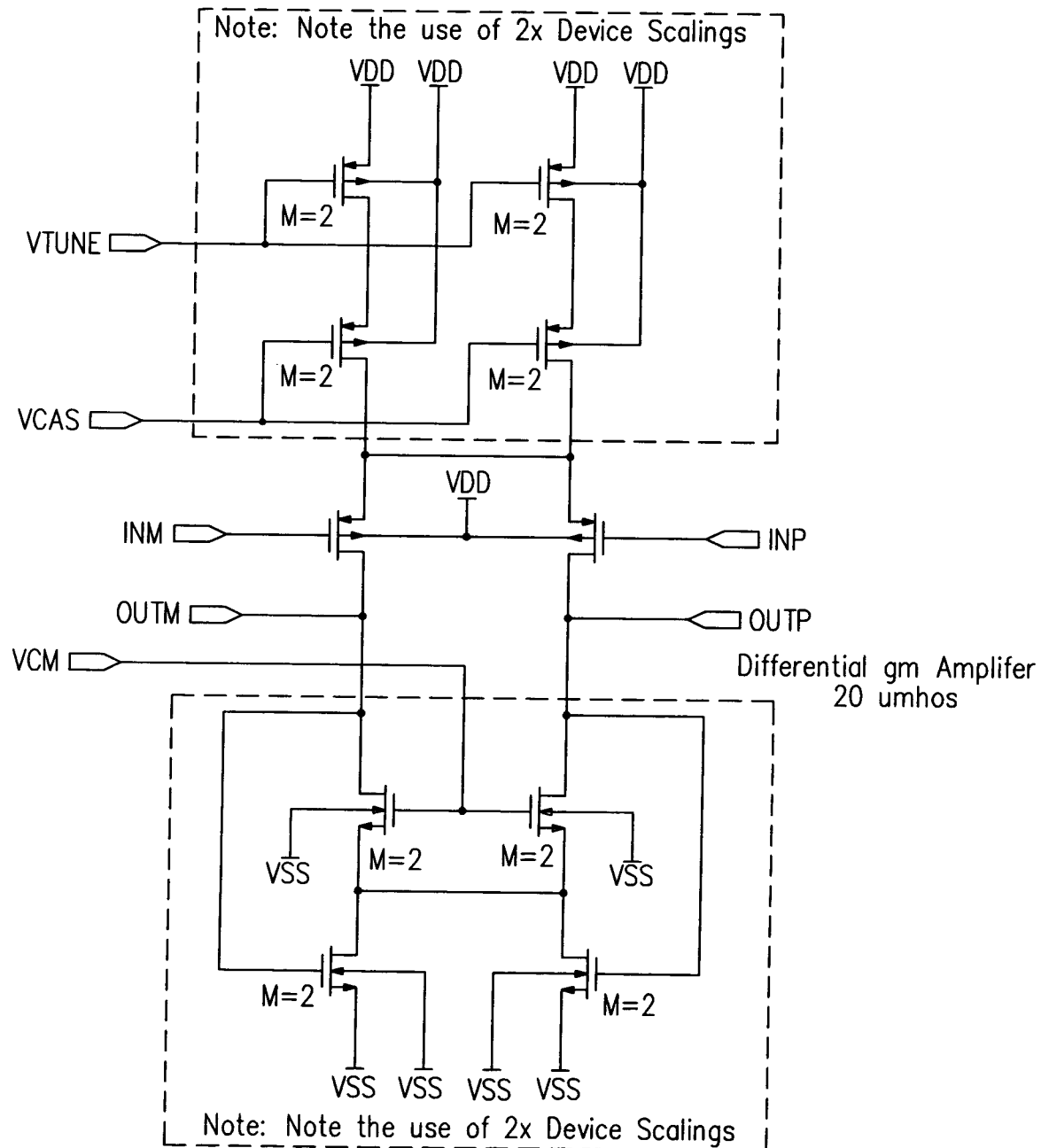


FIG. 11

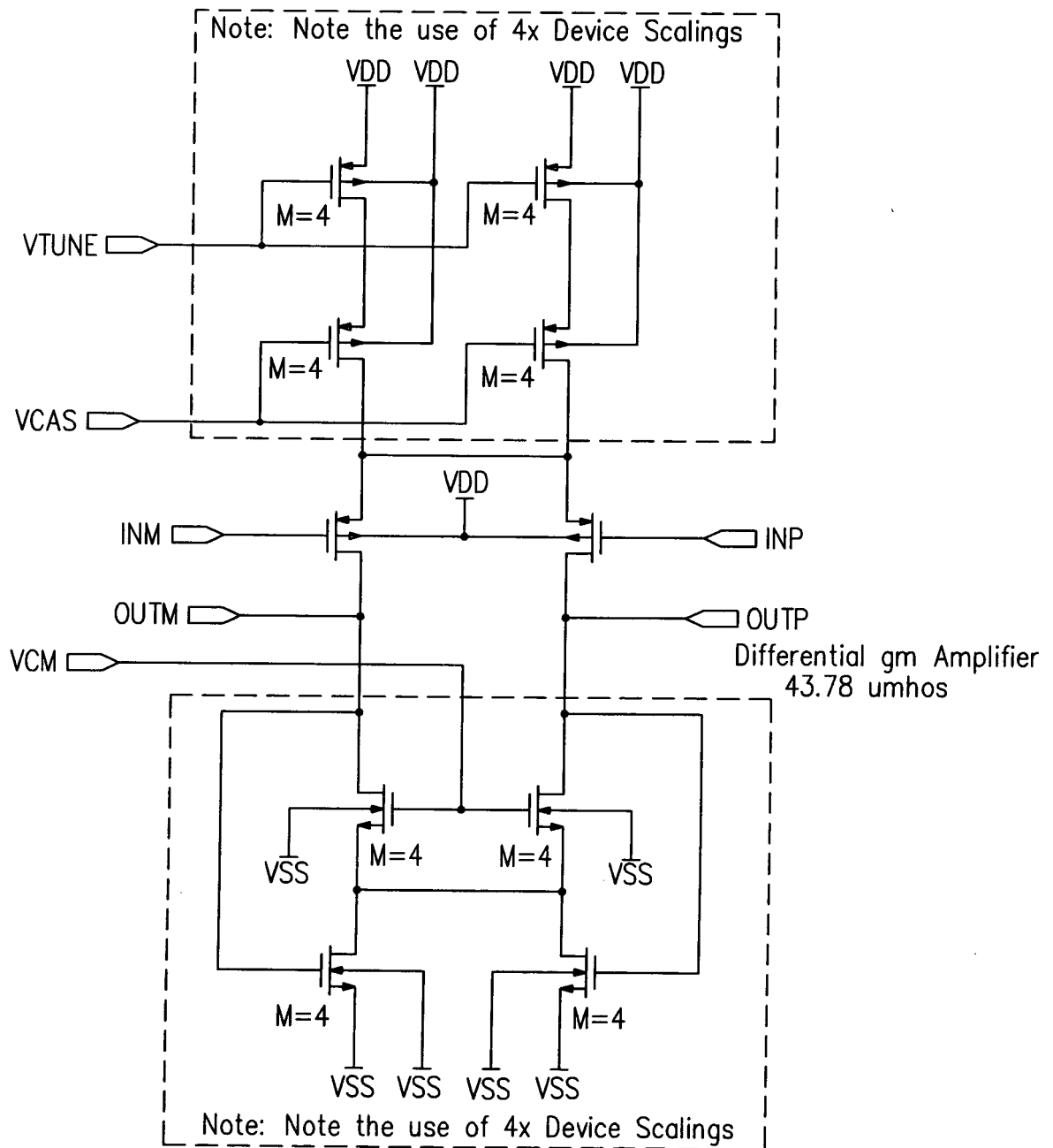


FIG. 12

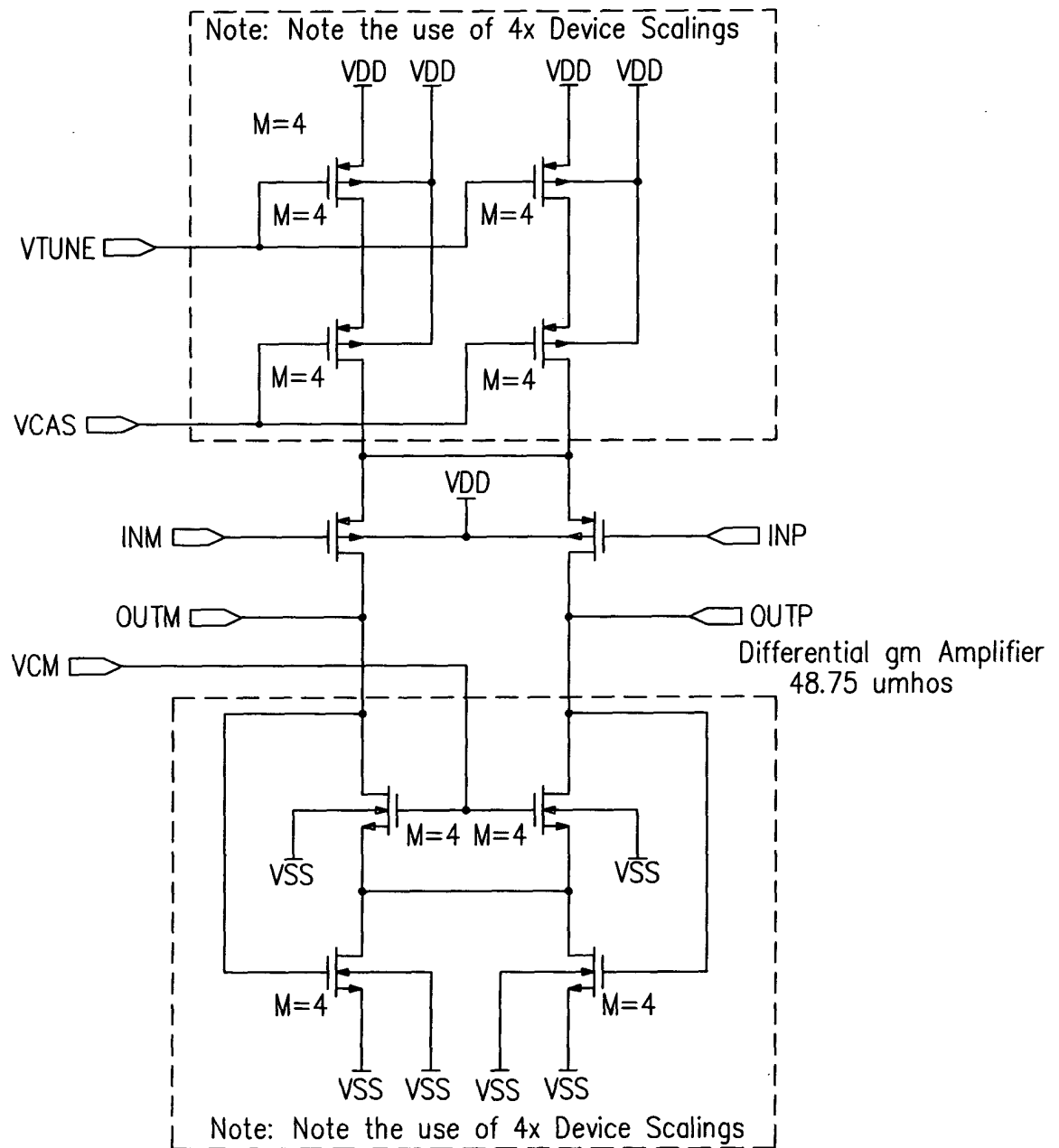


FIG. 13

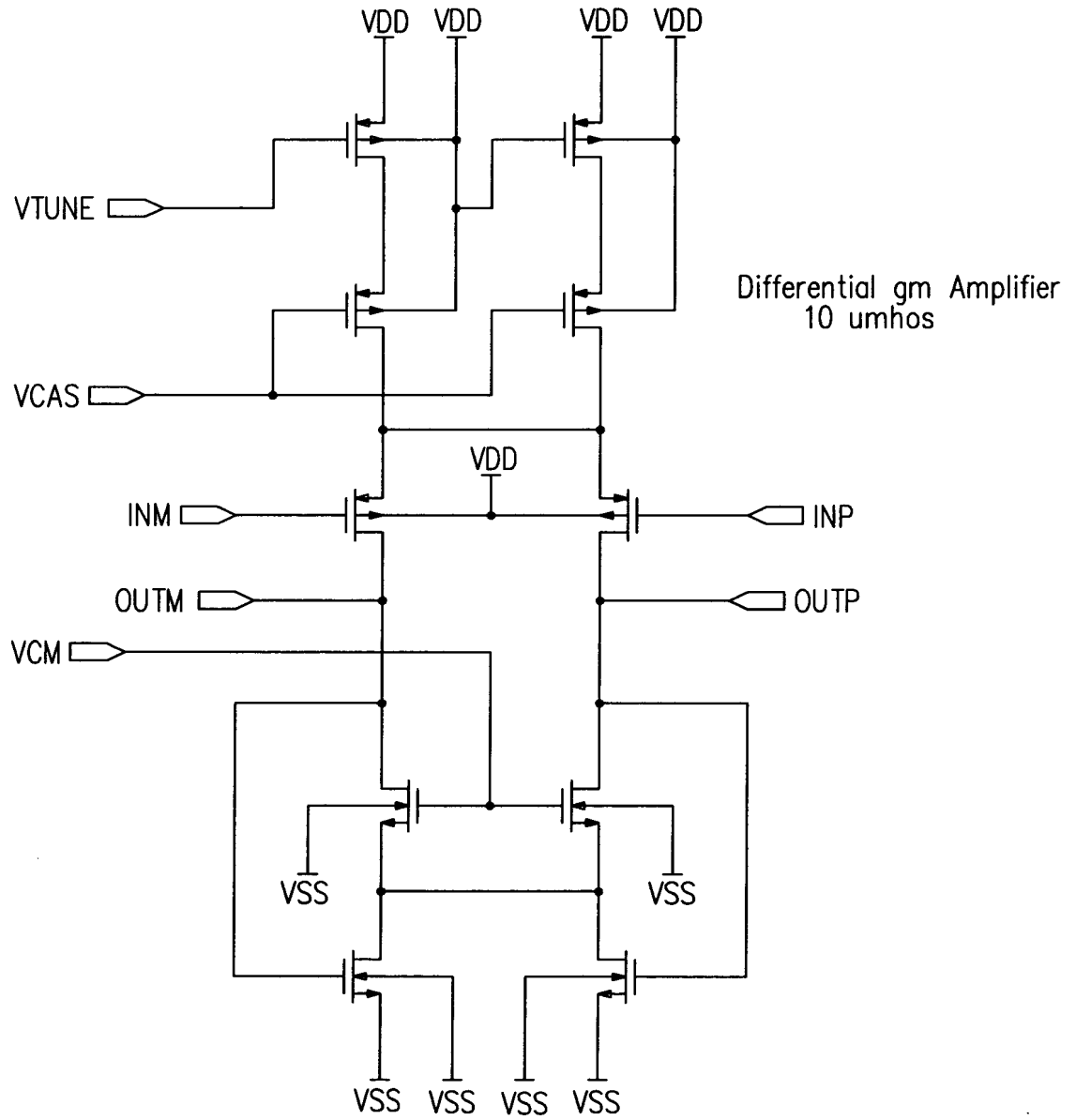


FIG. 14

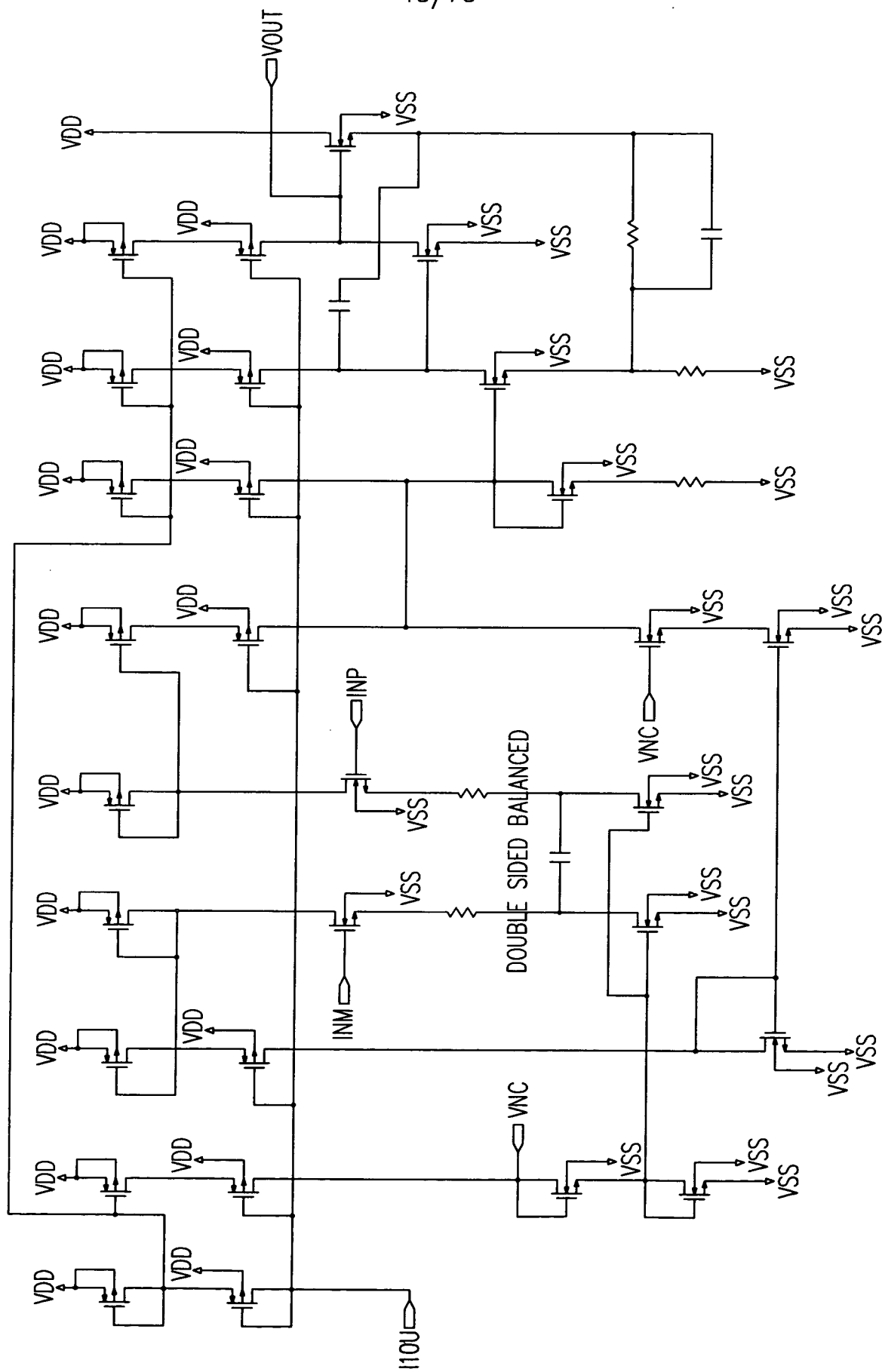


FIG. 15

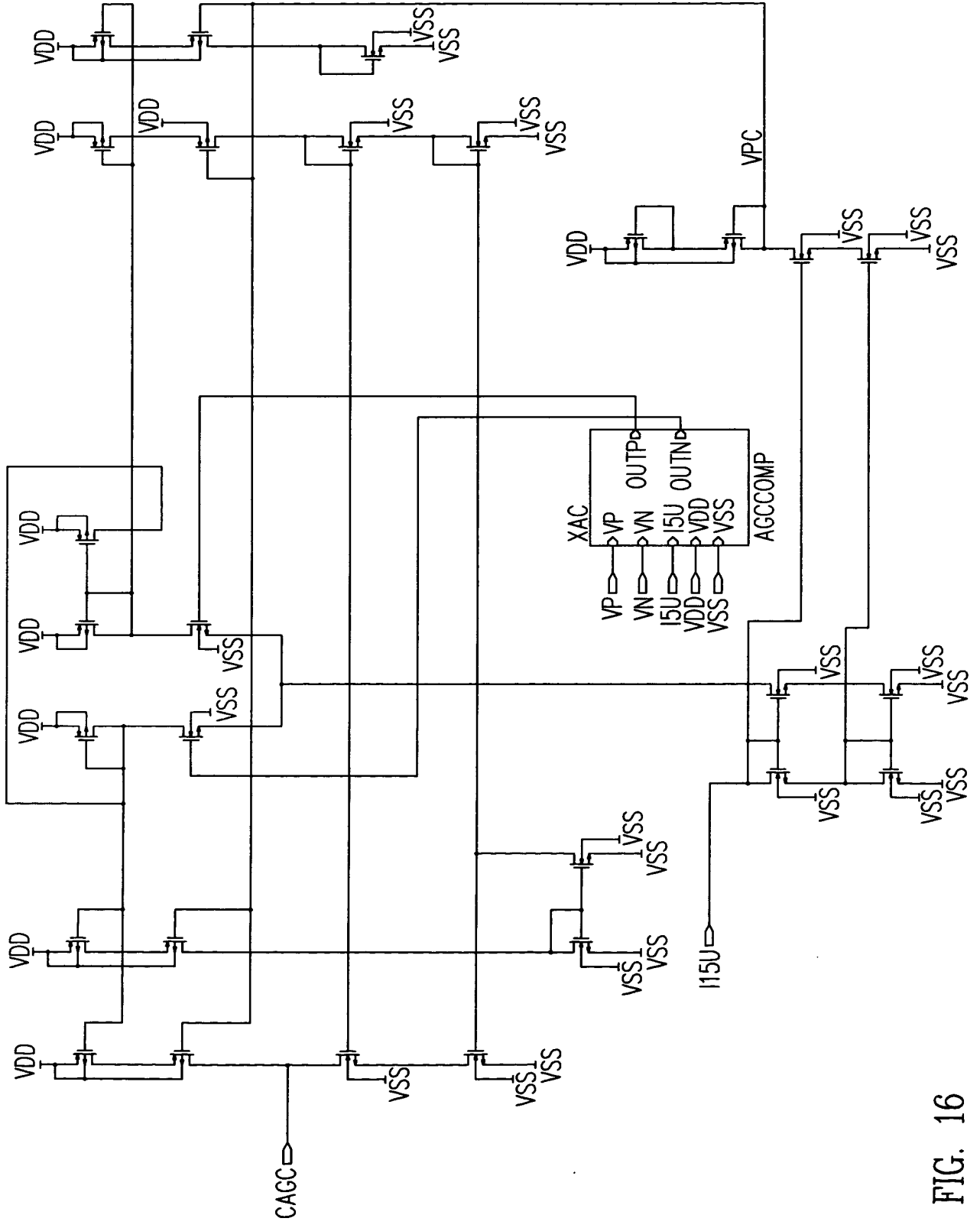
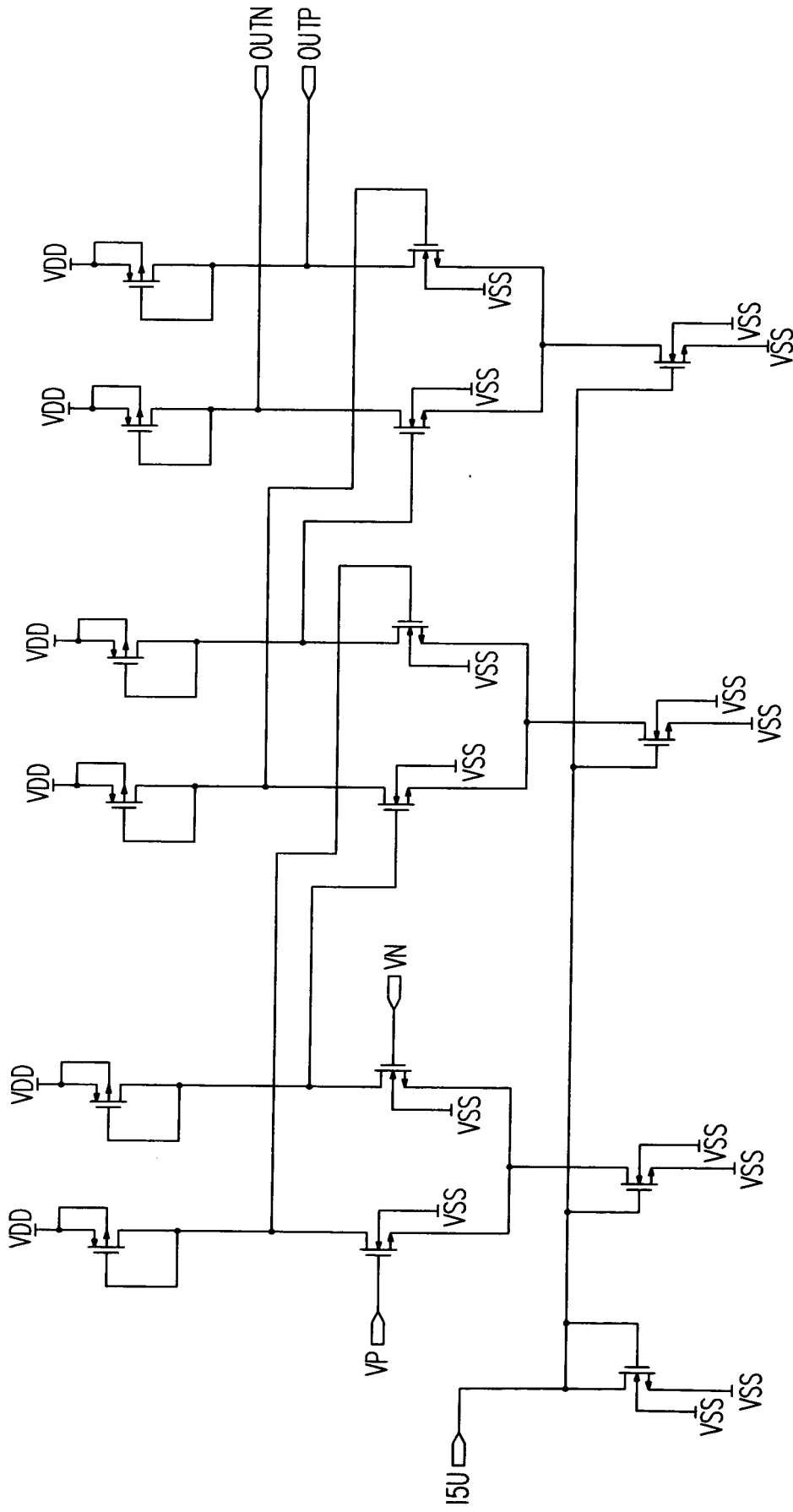


FIG. 16



AGC CONTROL COMPARATOR

FIG. 17

FIG. 18A	FIG. 18B
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KEY TO FIG. 18

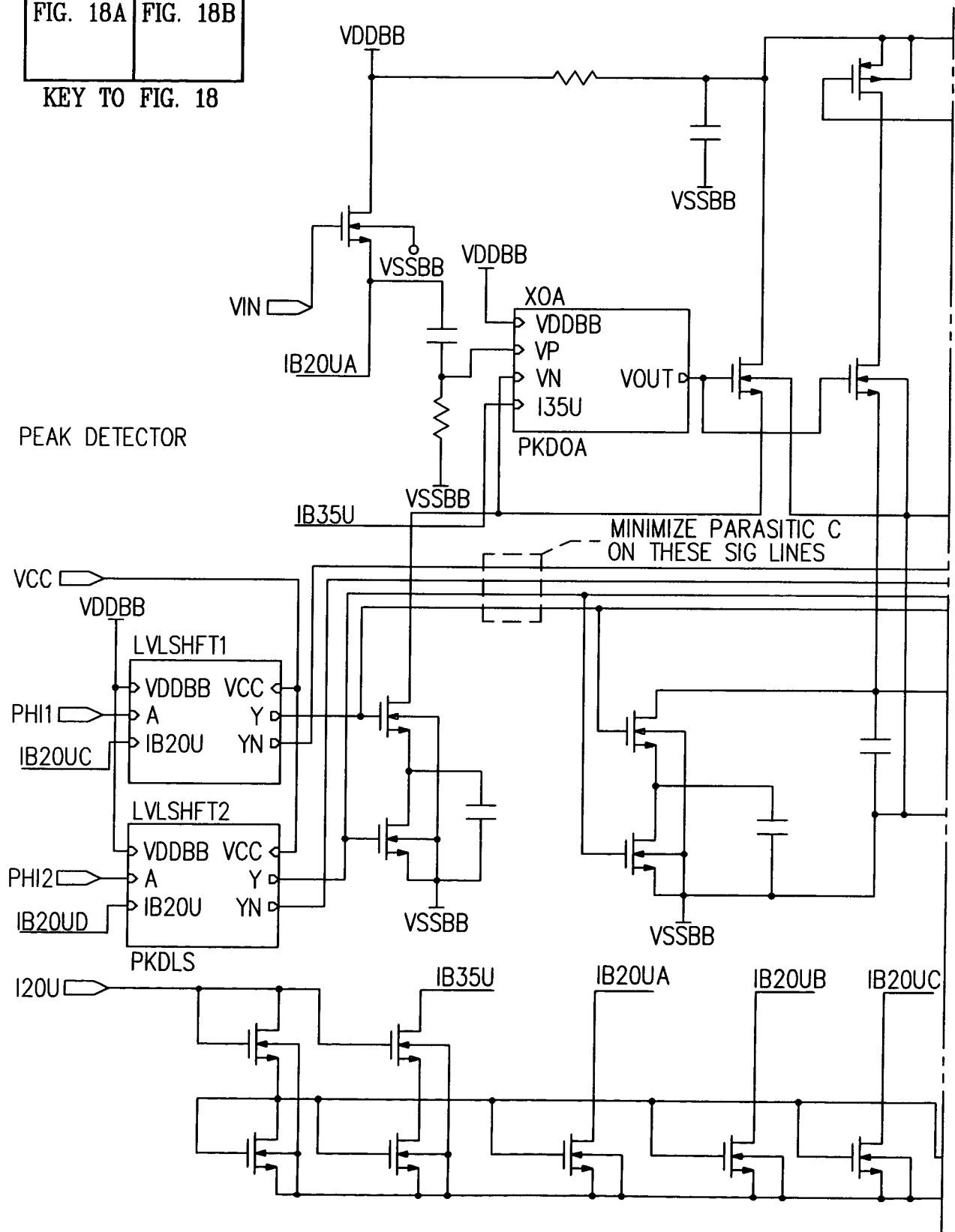


FIG. 18A

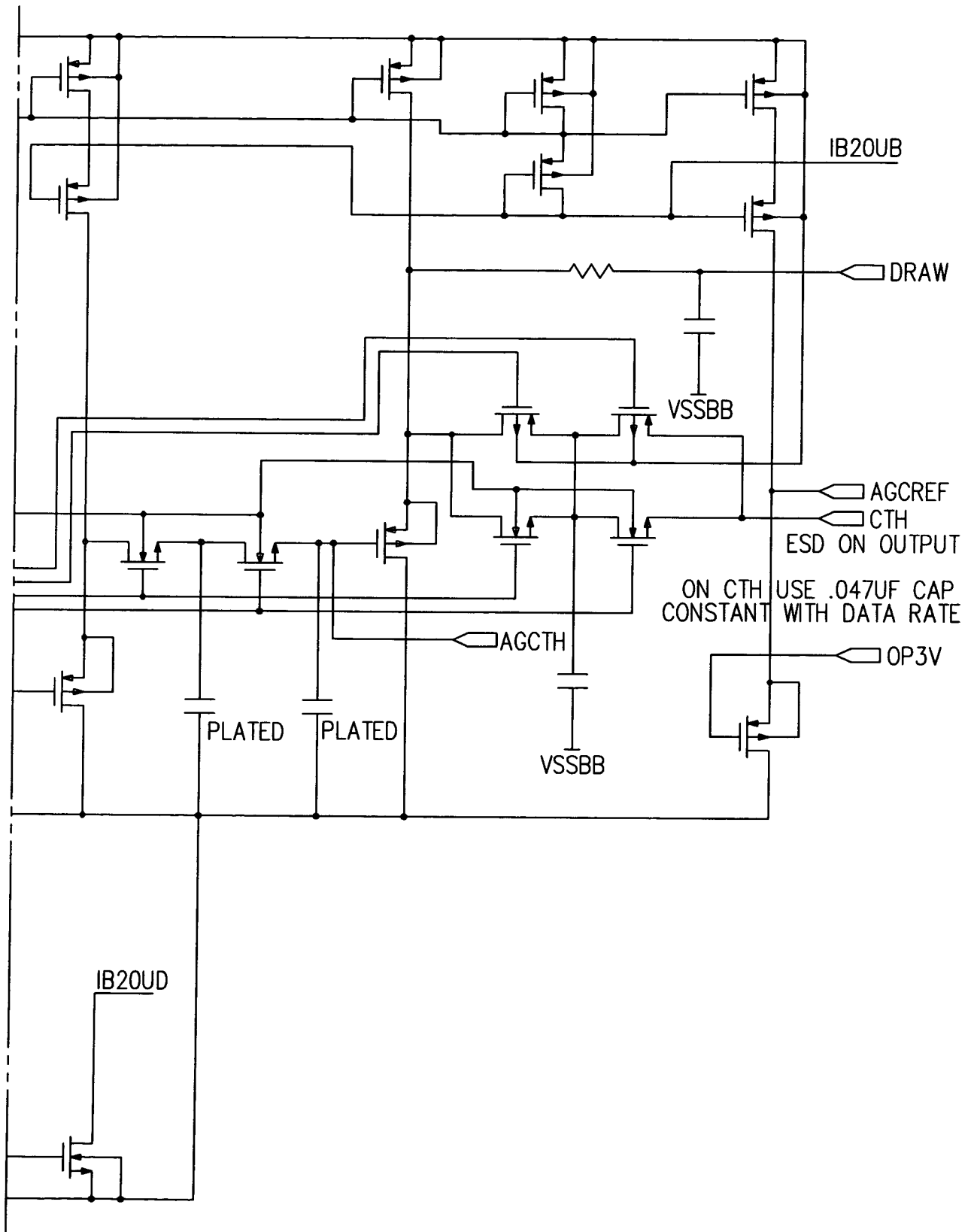


FIG. 18B

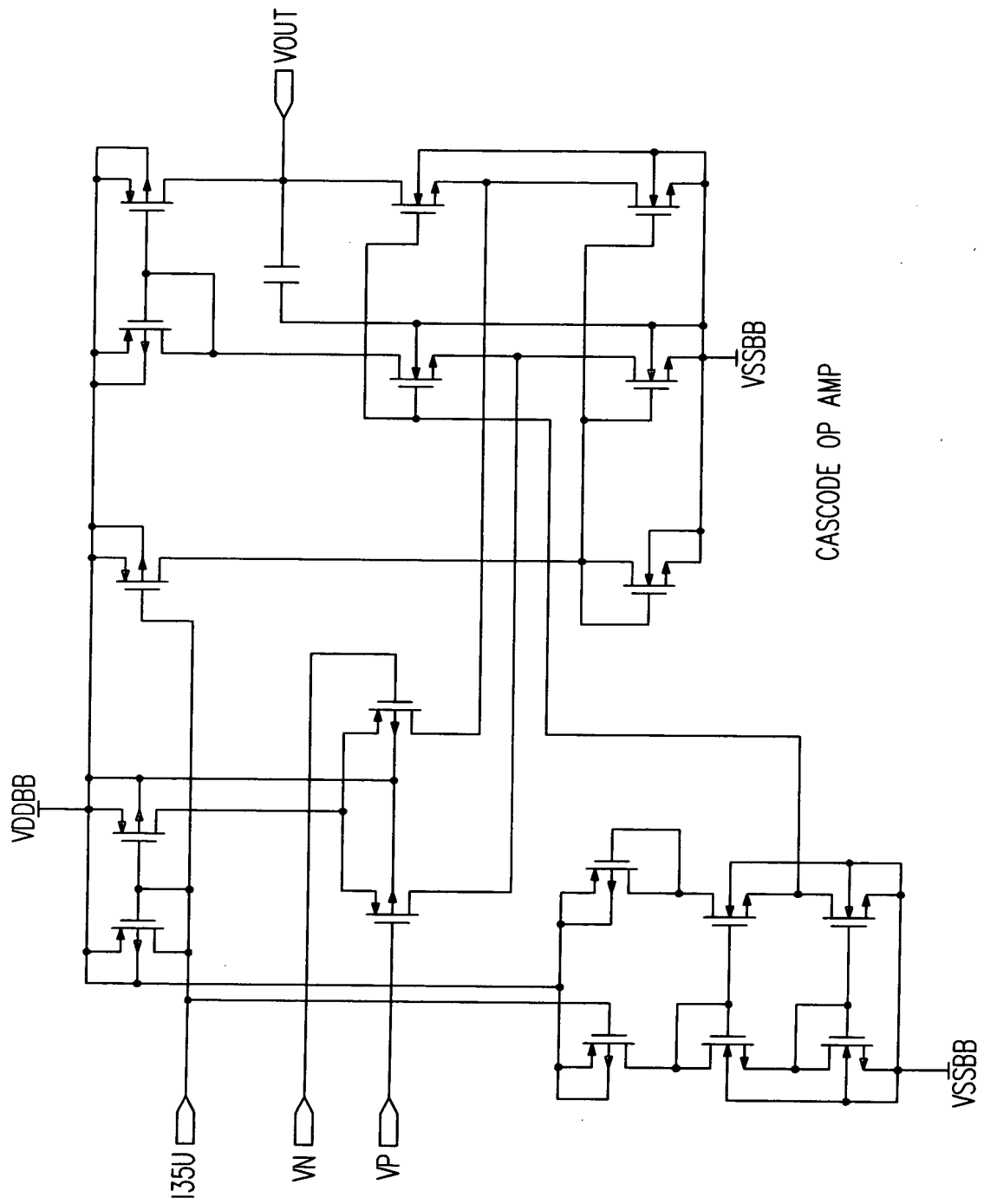


FIG. 19

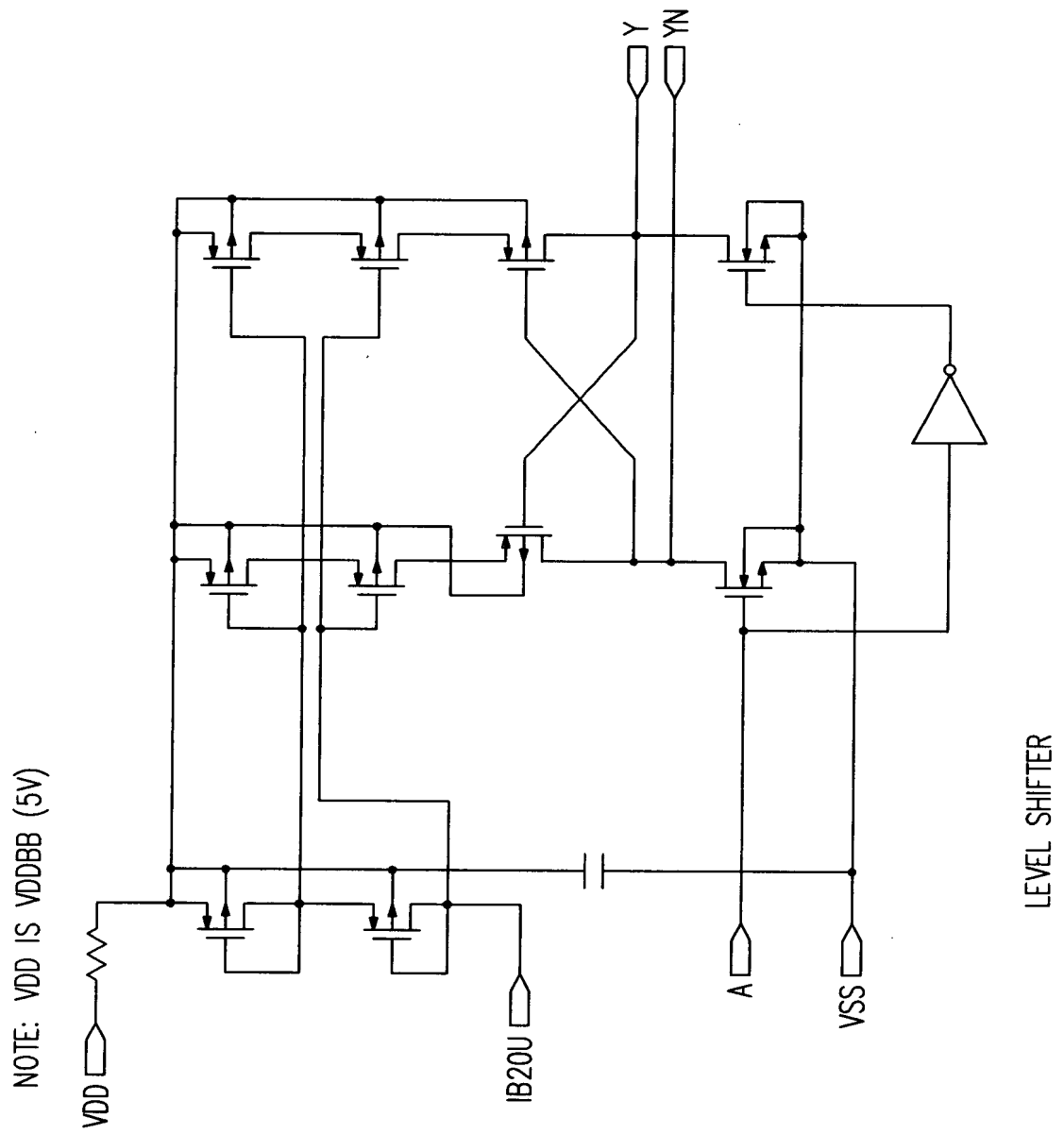


FIG. 20

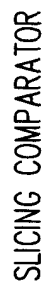


FIG. 21

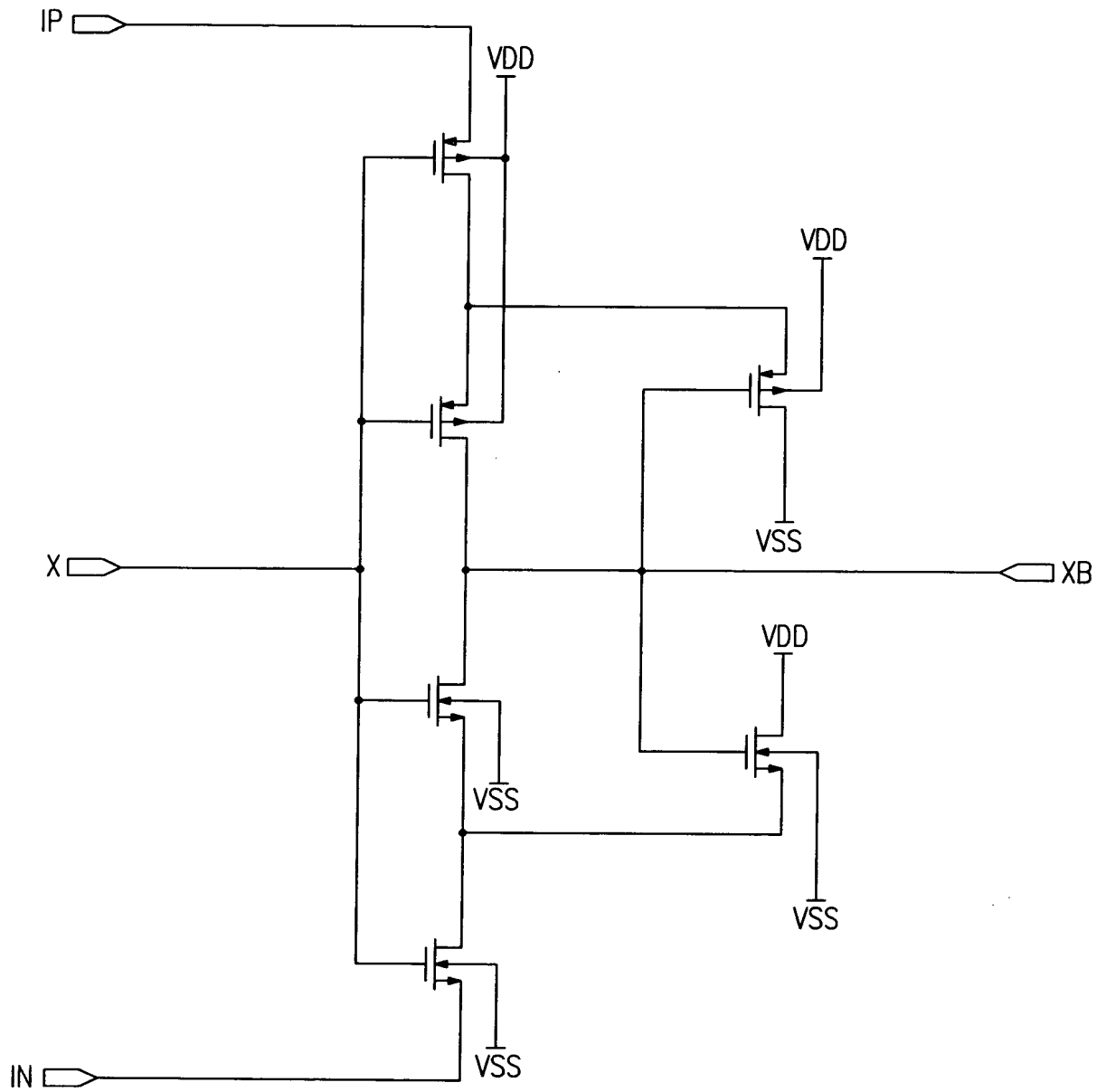


FIG. 22

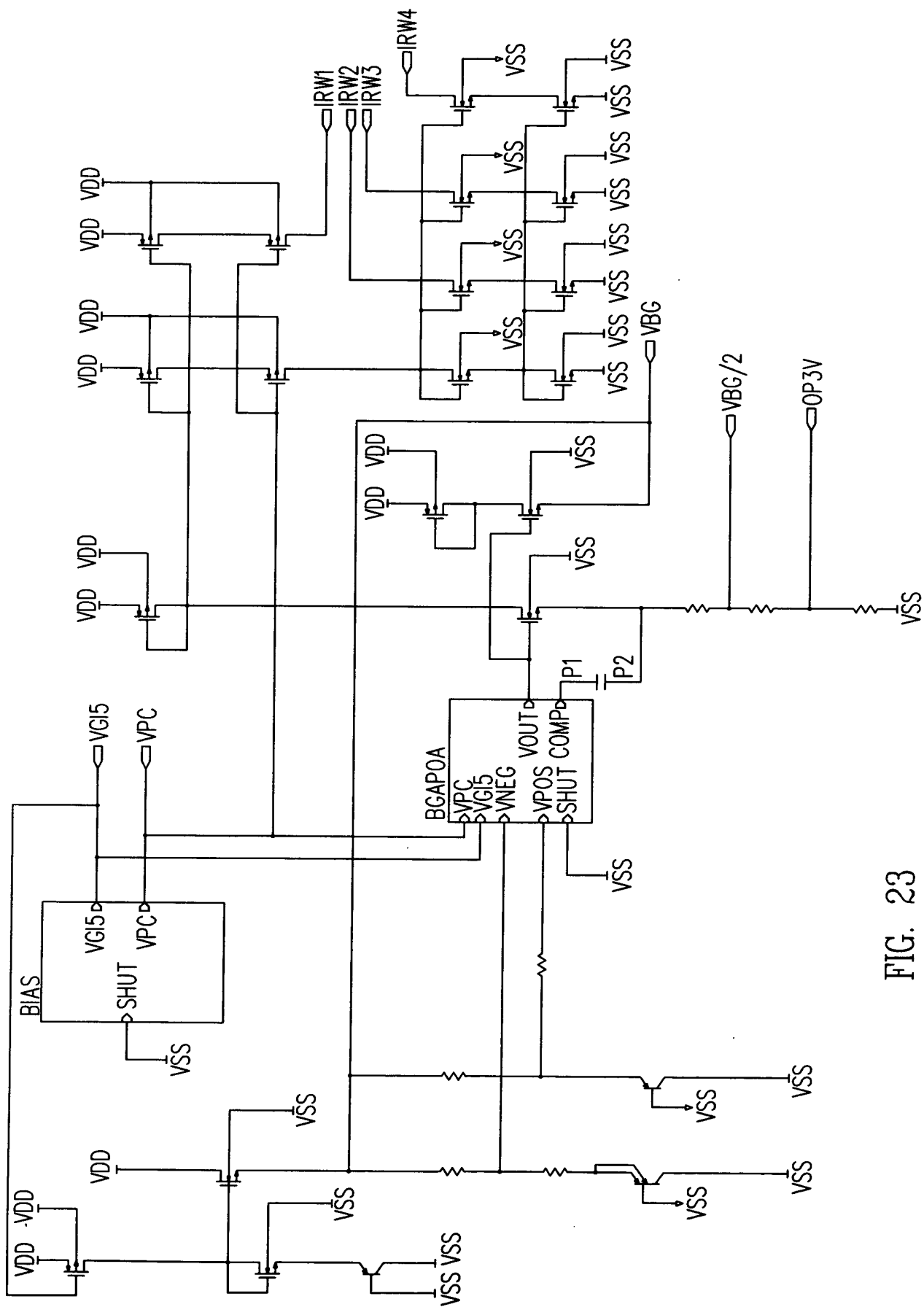


FIG. 23

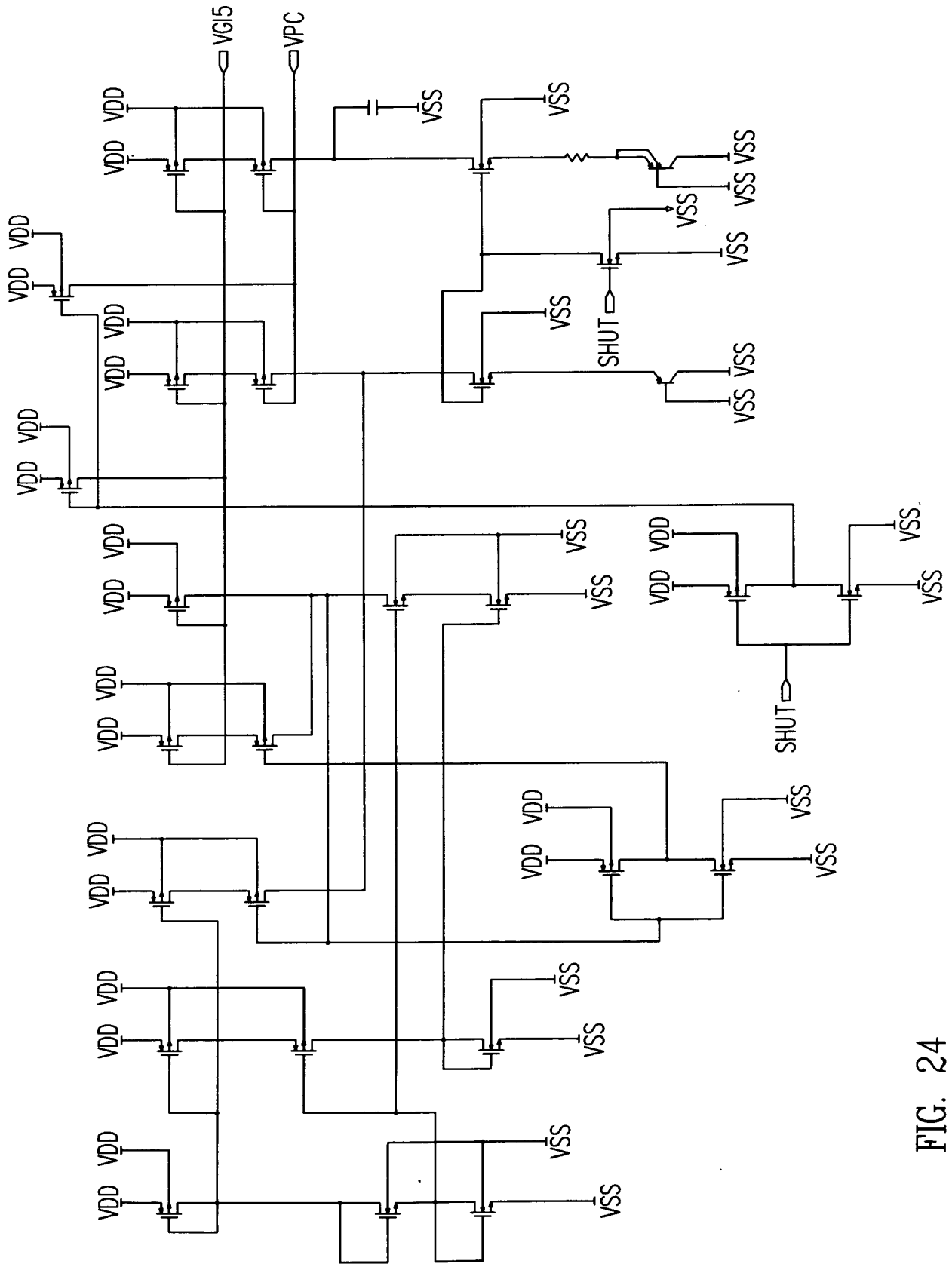


FIG. 24

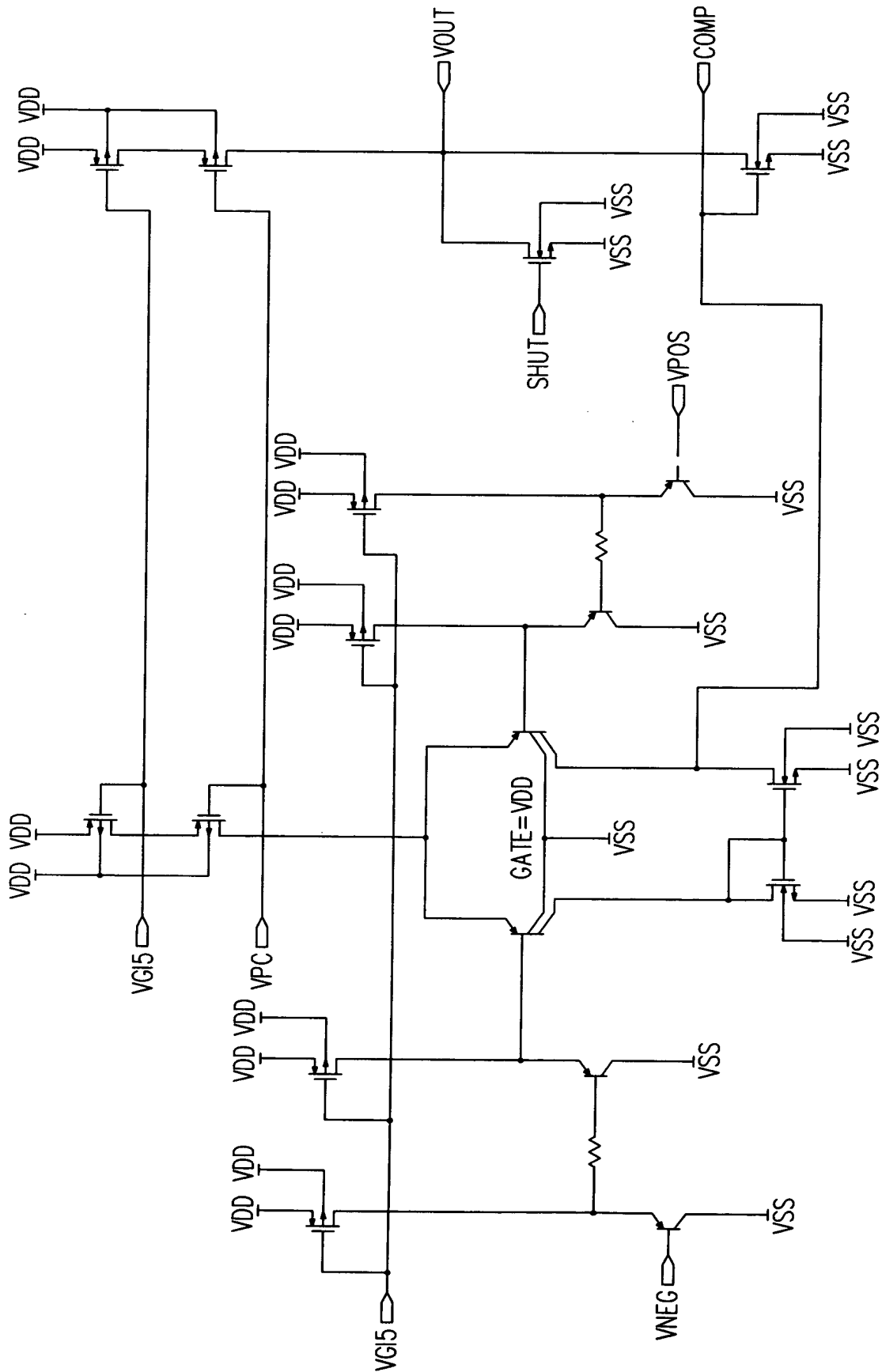


FIG. 25

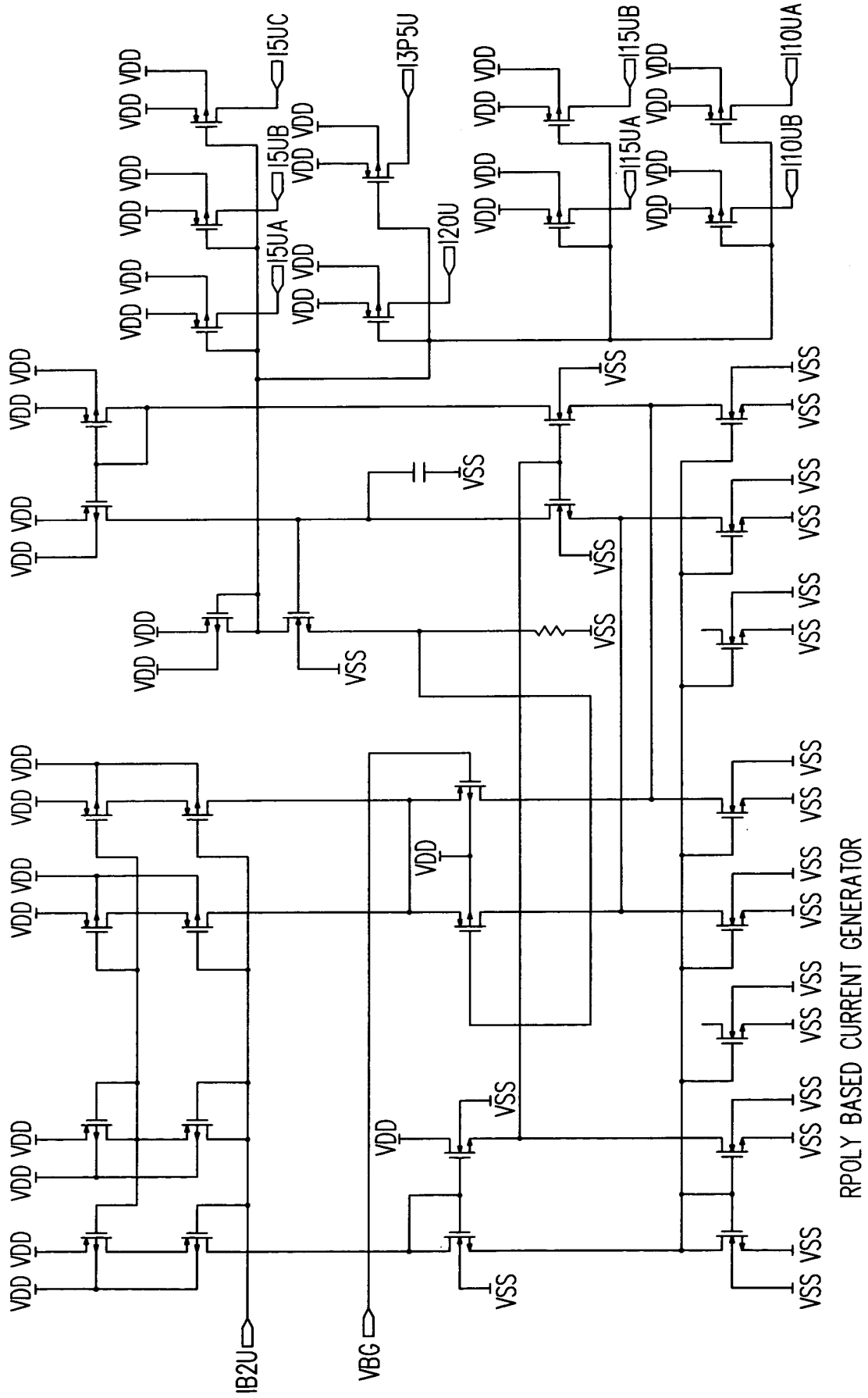


FIG. 26

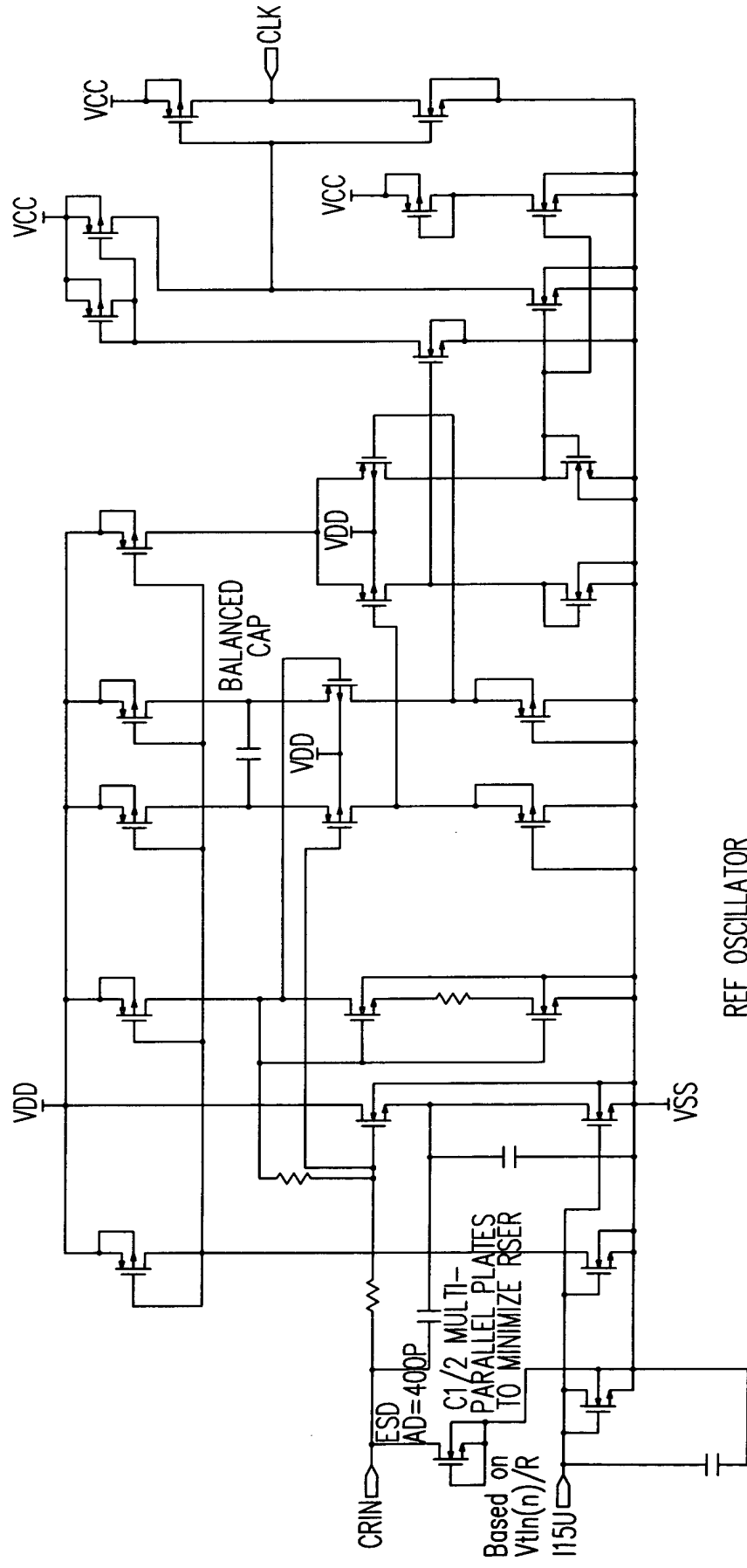


FIG. 27

NOTE: SIG DELAY THRU XS1 MUST BE LESS THAN
OR EQUAL TO SIG DELAY THRU XS2
ALL LOGIC USES VCC (2VT) SUPPLY

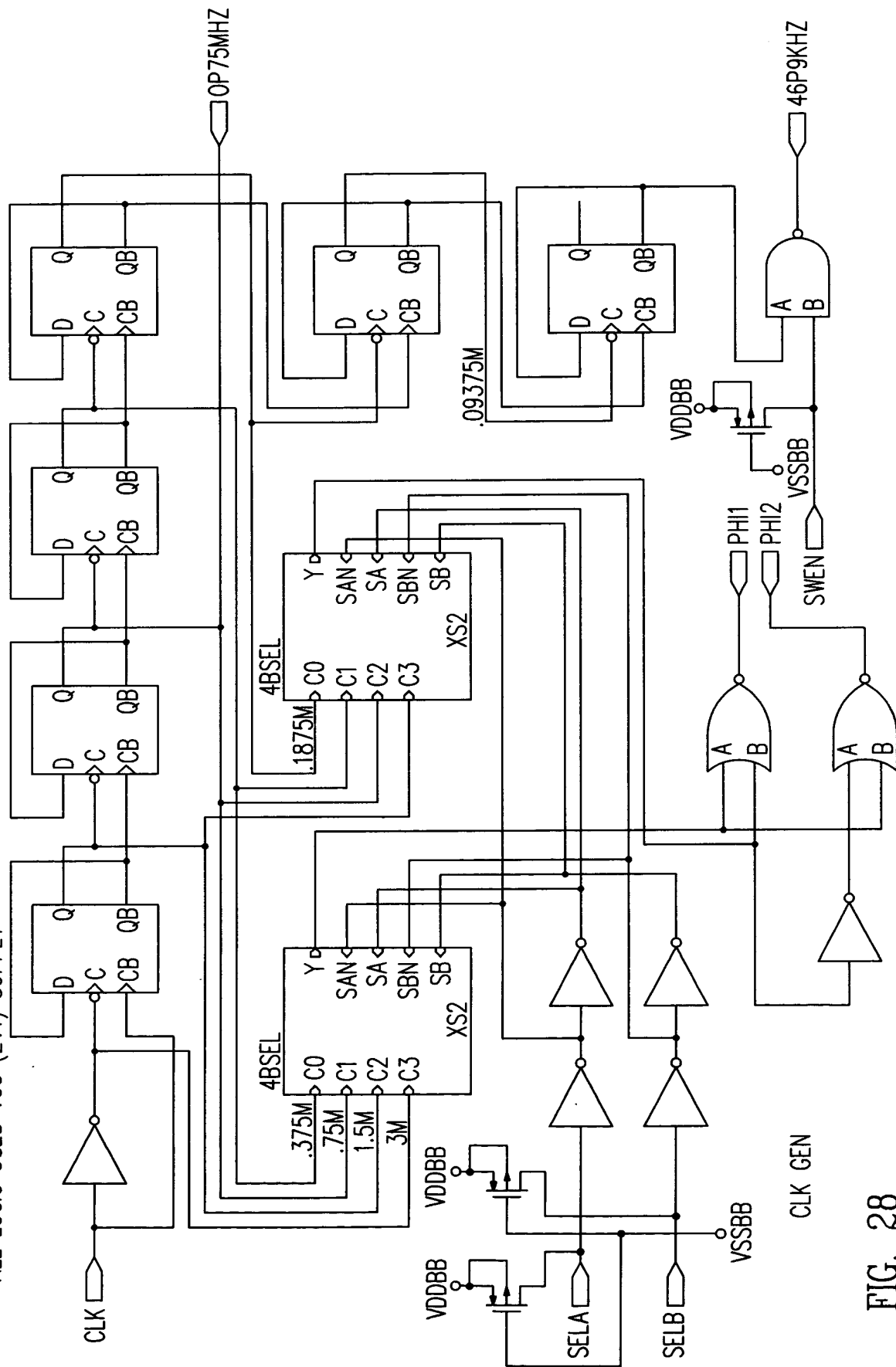


FIG. 28

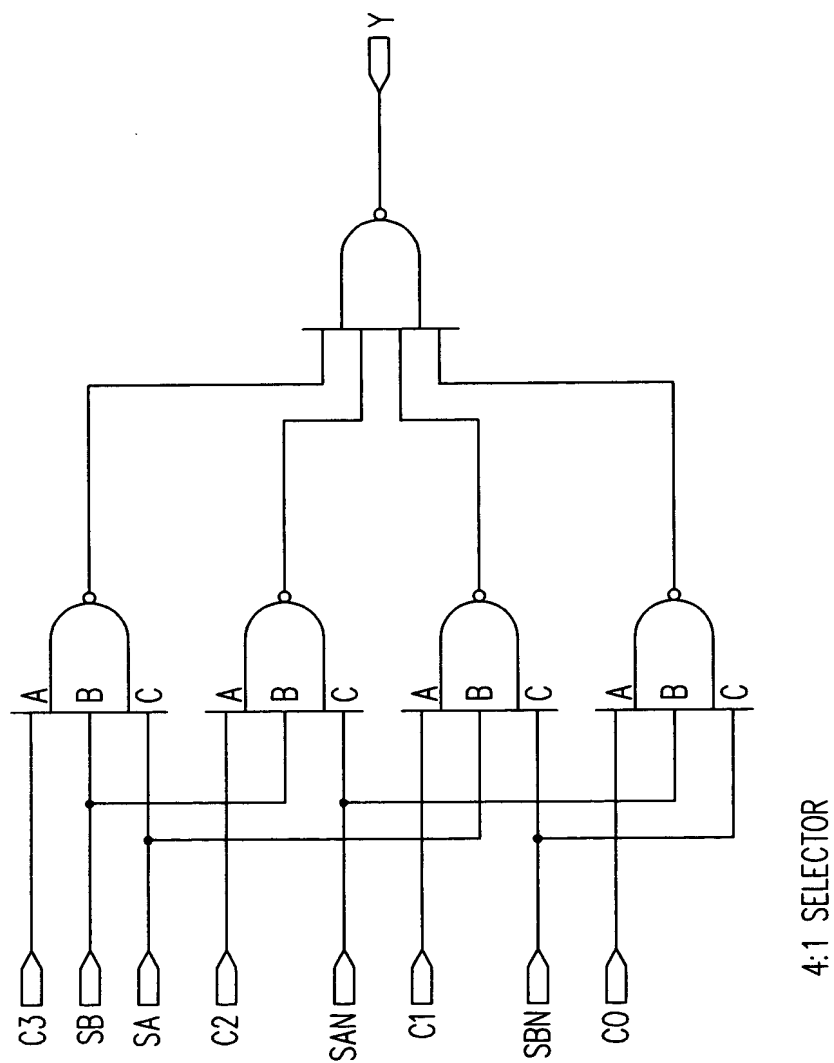


FIG. 29

Notes:

1. $I_{poly} \Rightarrow V_{bg}/R_{poly}$ is used to bias the comparator since this current has the least spread: 2.5:1
2. $I_{rwell} \Rightarrow V_{bg}/R_{well}$ is used to program a constant K in the PLL loop analysis
3. K is equivalent to the $gm \cdot R$ dc term in the PLL analysis. For this loop $K = 0.375$

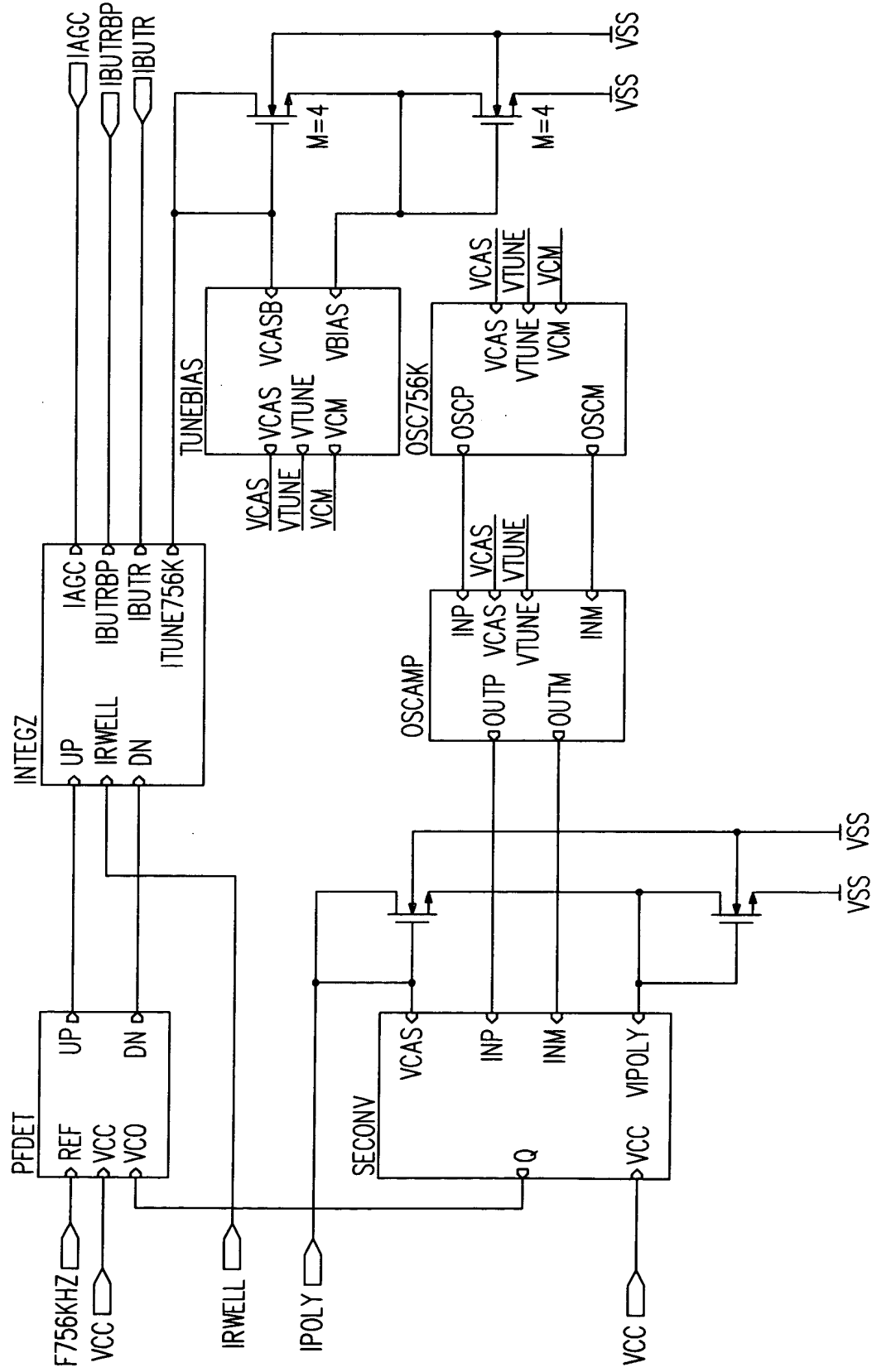
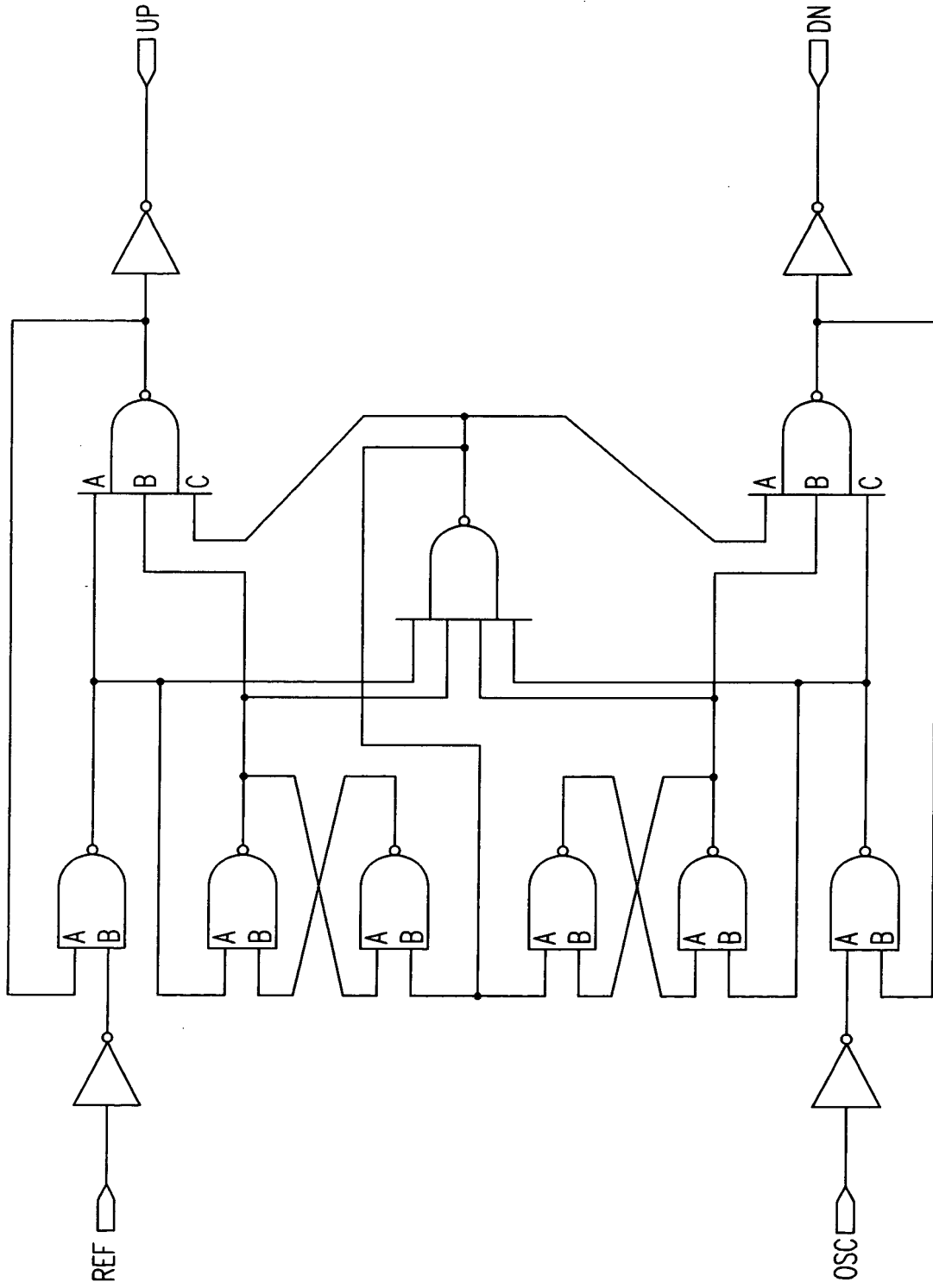


FIG. 30

755.81KHz Tuning Phase Locked Loop



VCC VCC is the P-Channel Power Supply

PHASE/FREQUENCY DETECTOR

FIG. 31

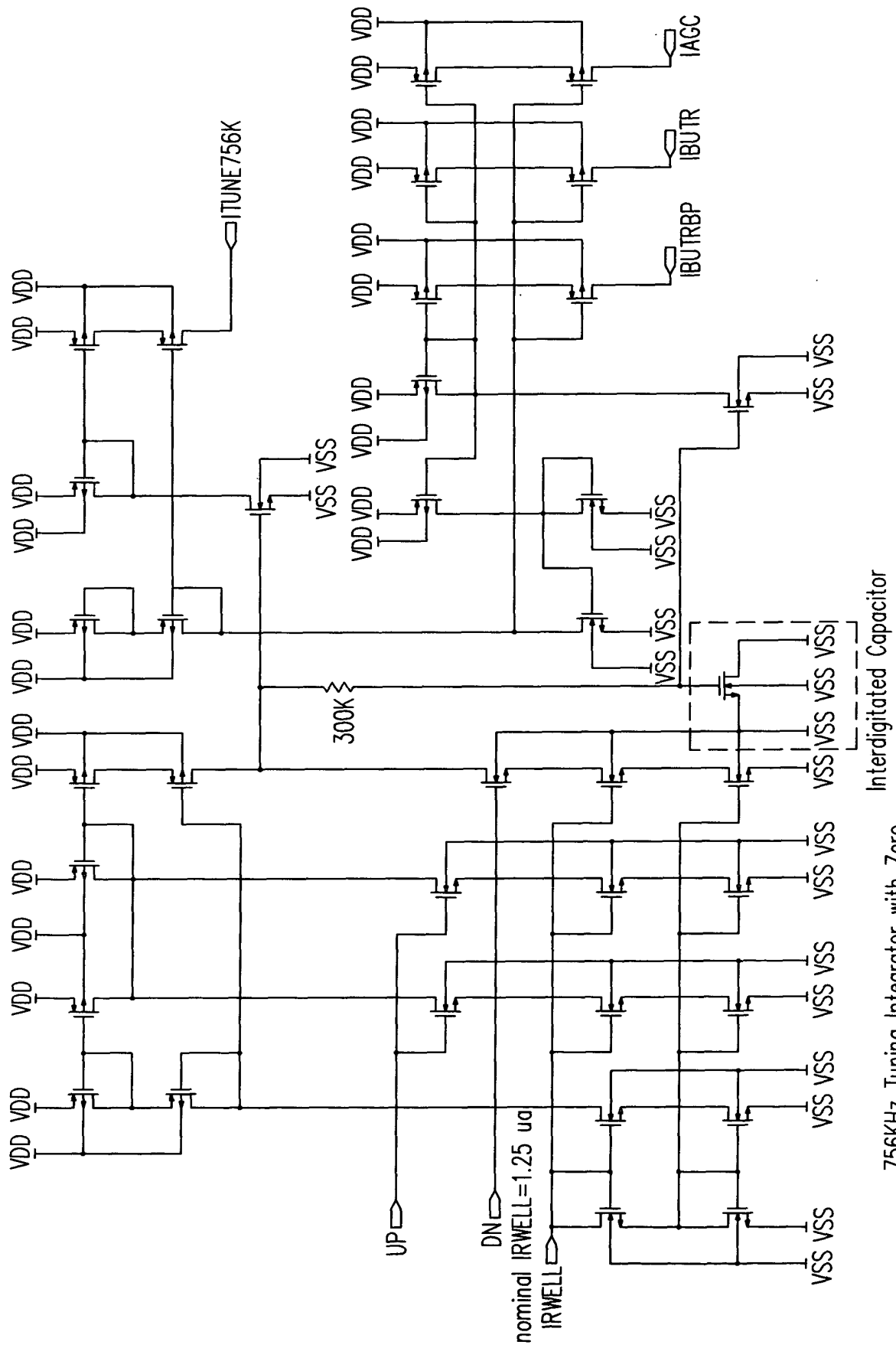
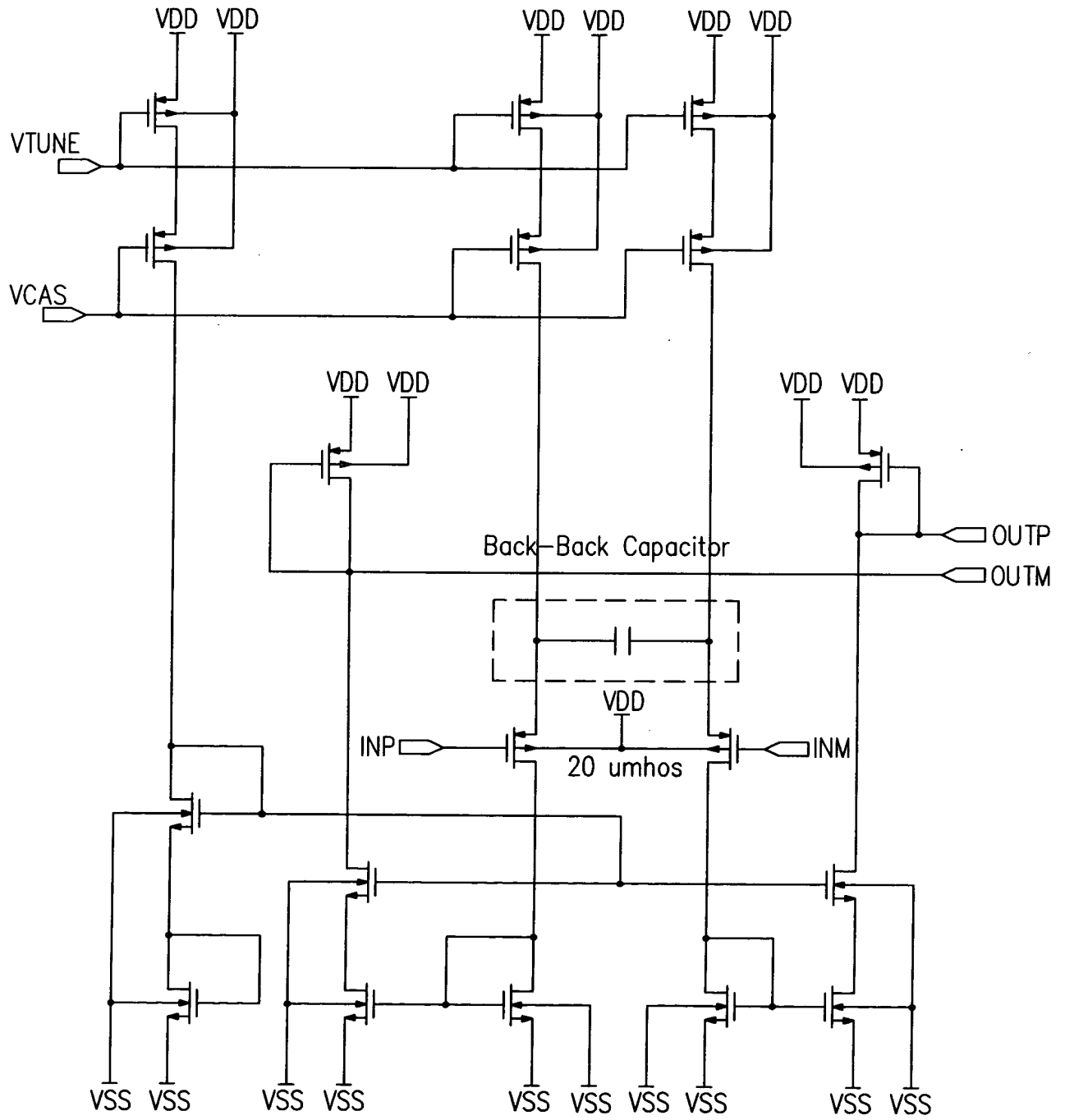


FIG. 32

FIG. 33



Differential AC-coupled Voltage Amplifier

FIG. 34

Tuning Bias Generator

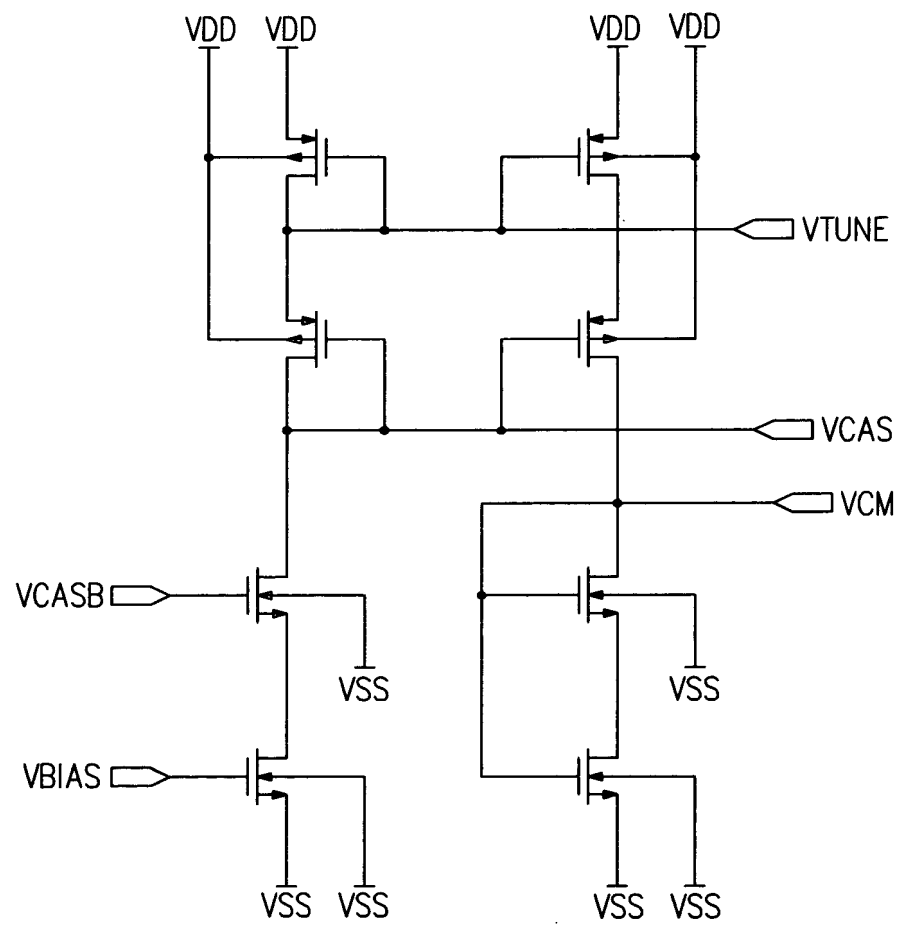


FIG. 35

755.81KHz Reference Oscillator for gm/C Tuning

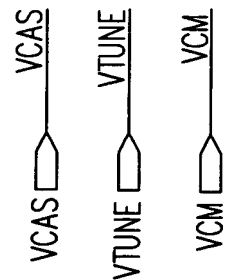
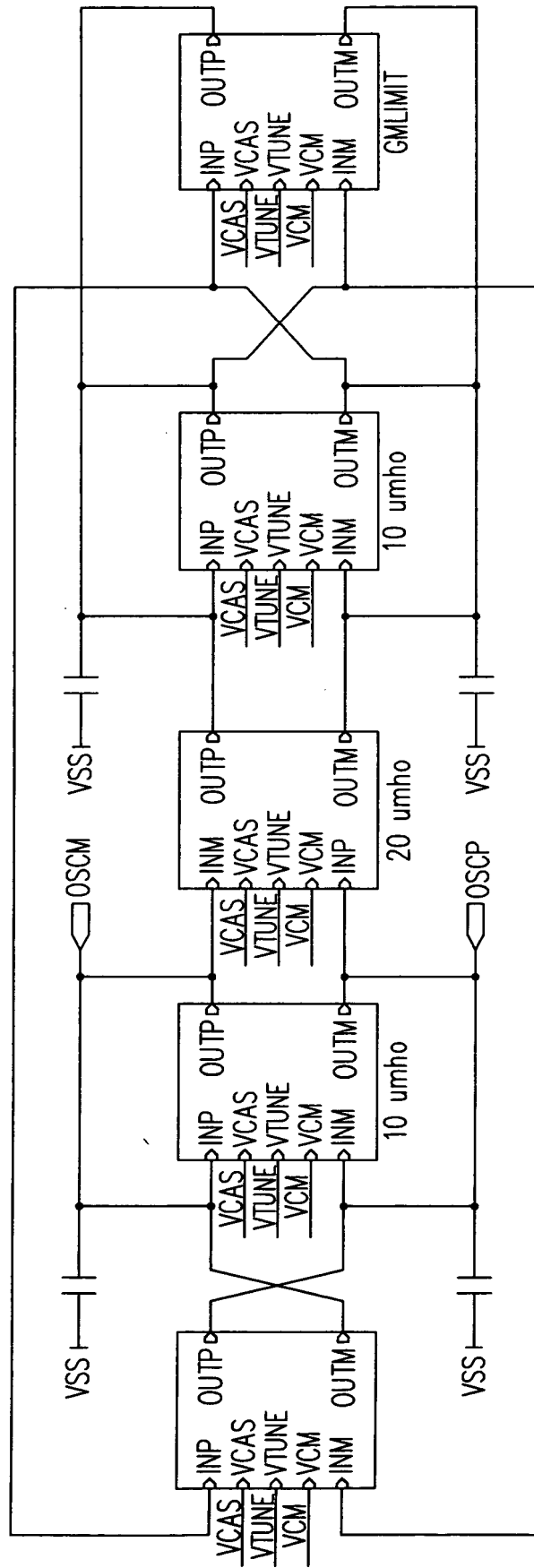


FIG. 36

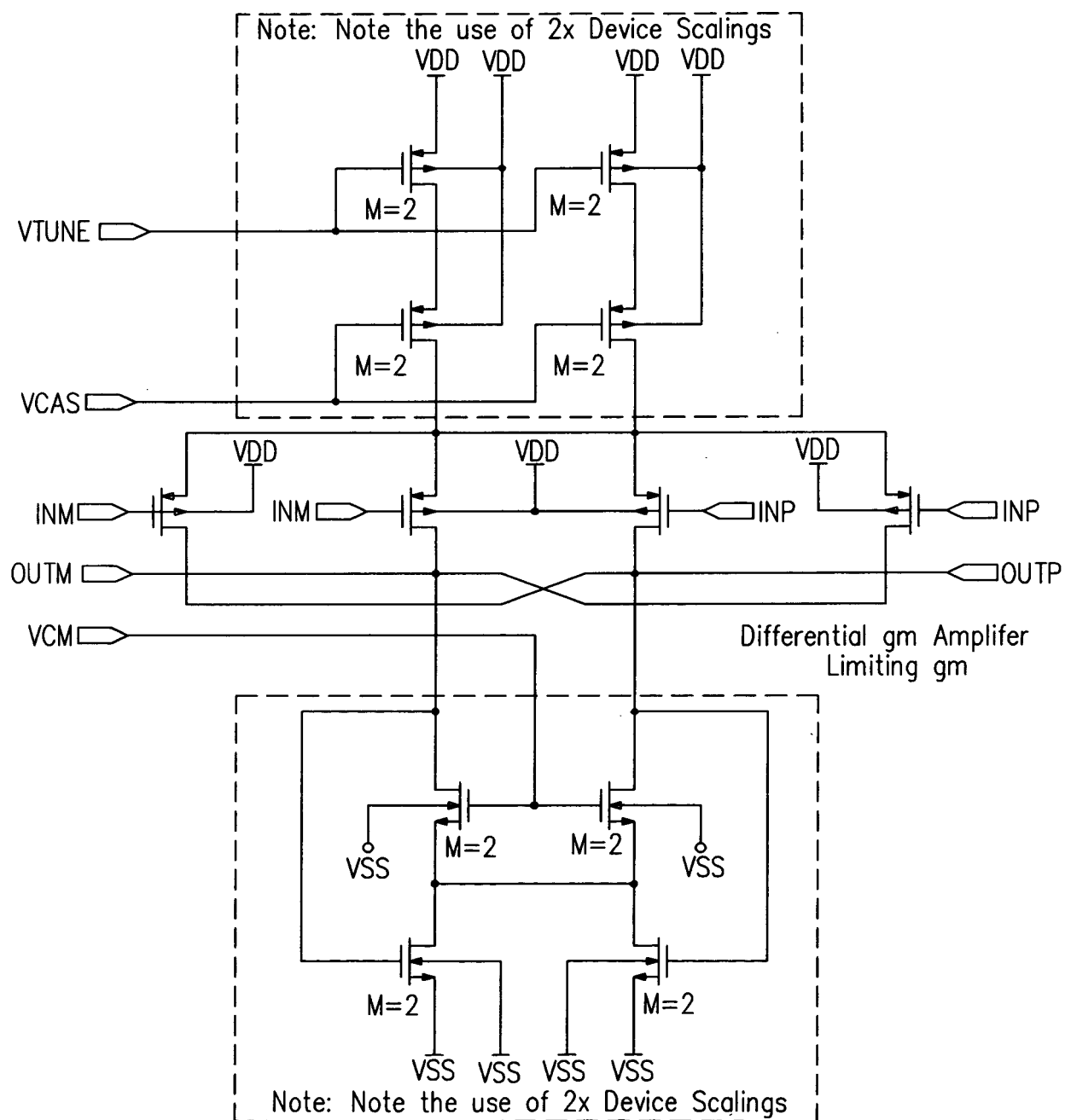
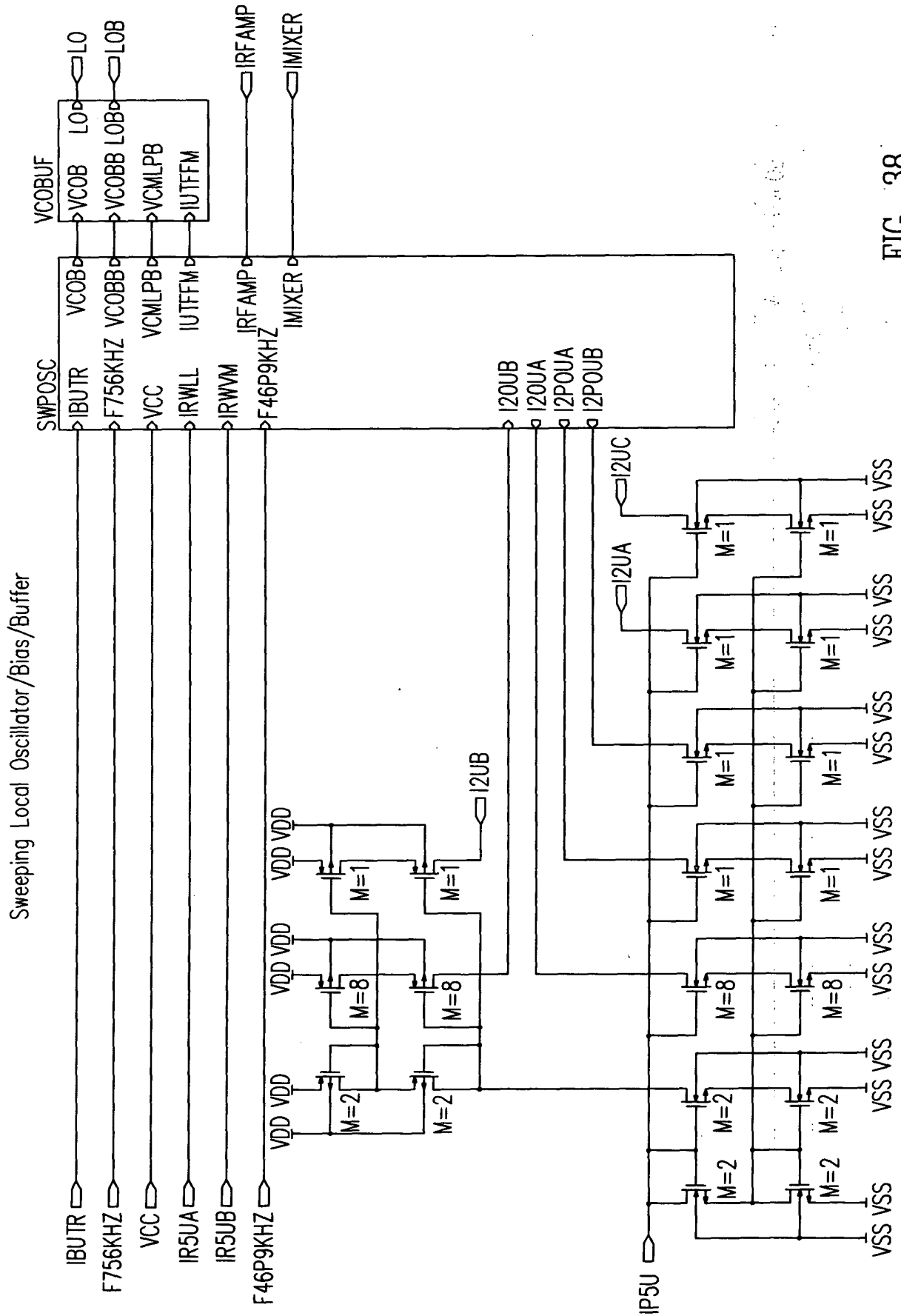
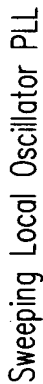


FIG. 37





Notes:

1. $\text{lbutr} \Rightarrow \text{lbutr}$ is the tuning Butterworth filter tuning current

FIG. 40

FIG. 41A	FIG. 41B
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KEY TO FIG. 41

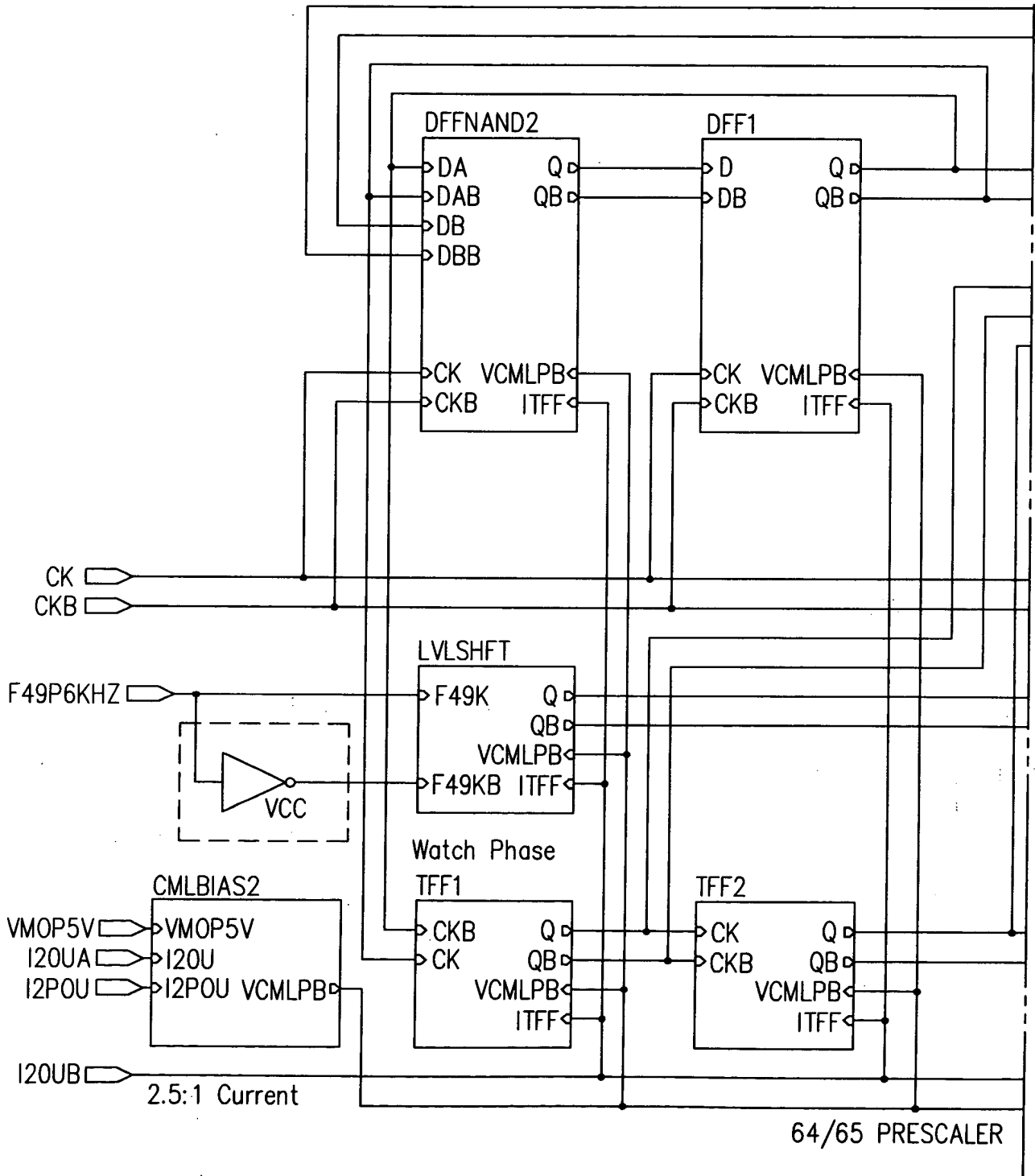


FIG. 41A

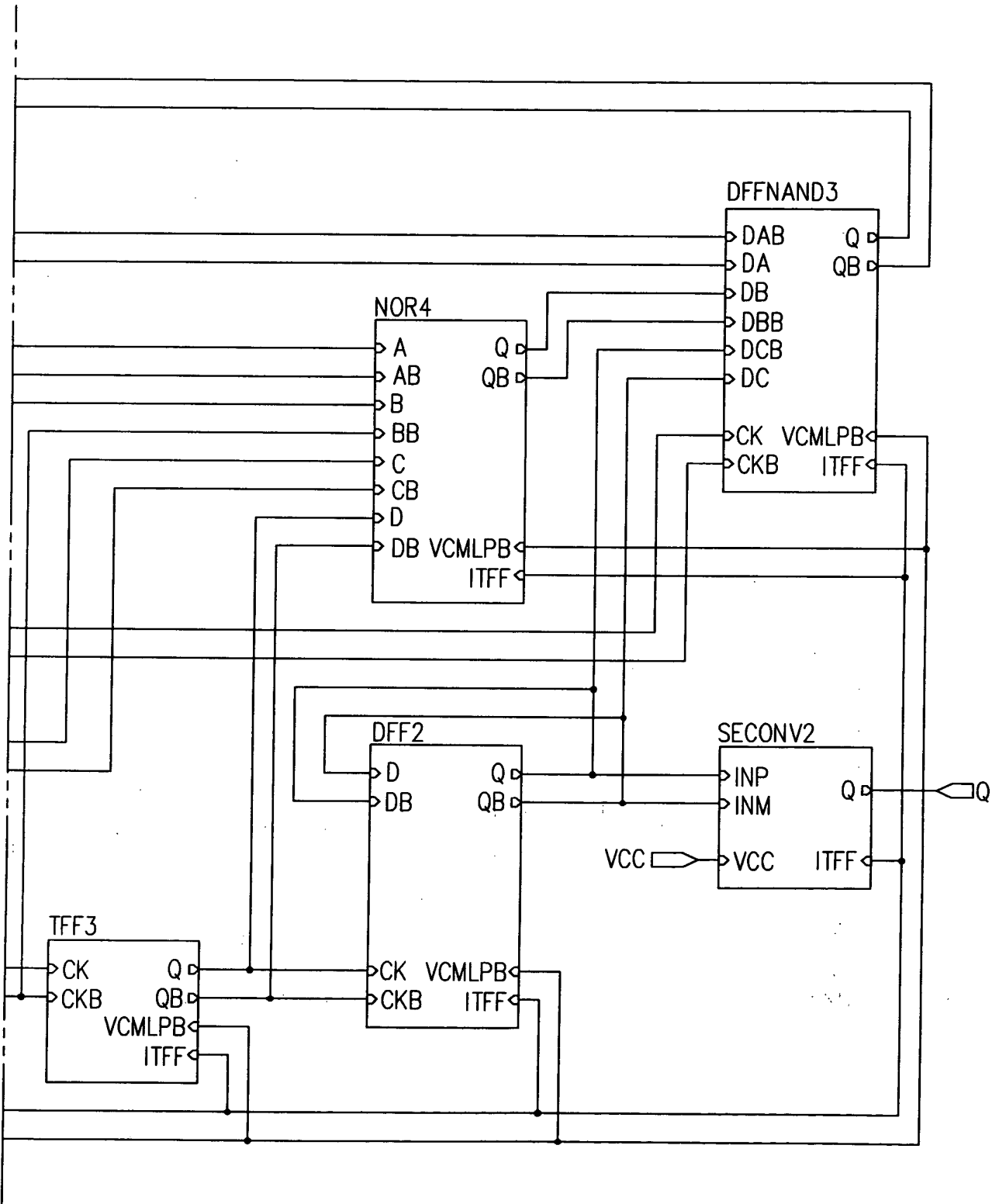
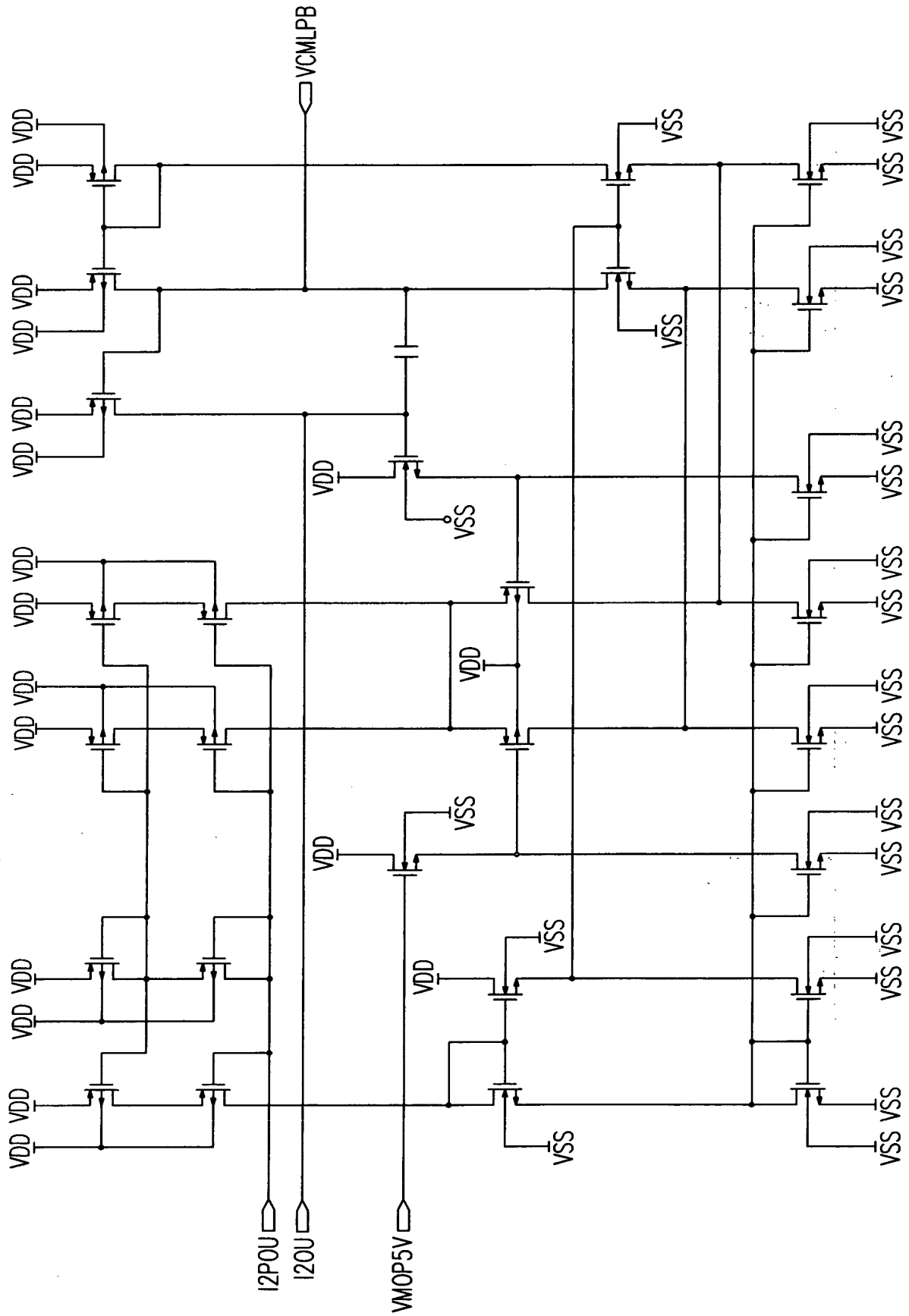


FIG. 41B



CML Bias for 64/65 Prescaler

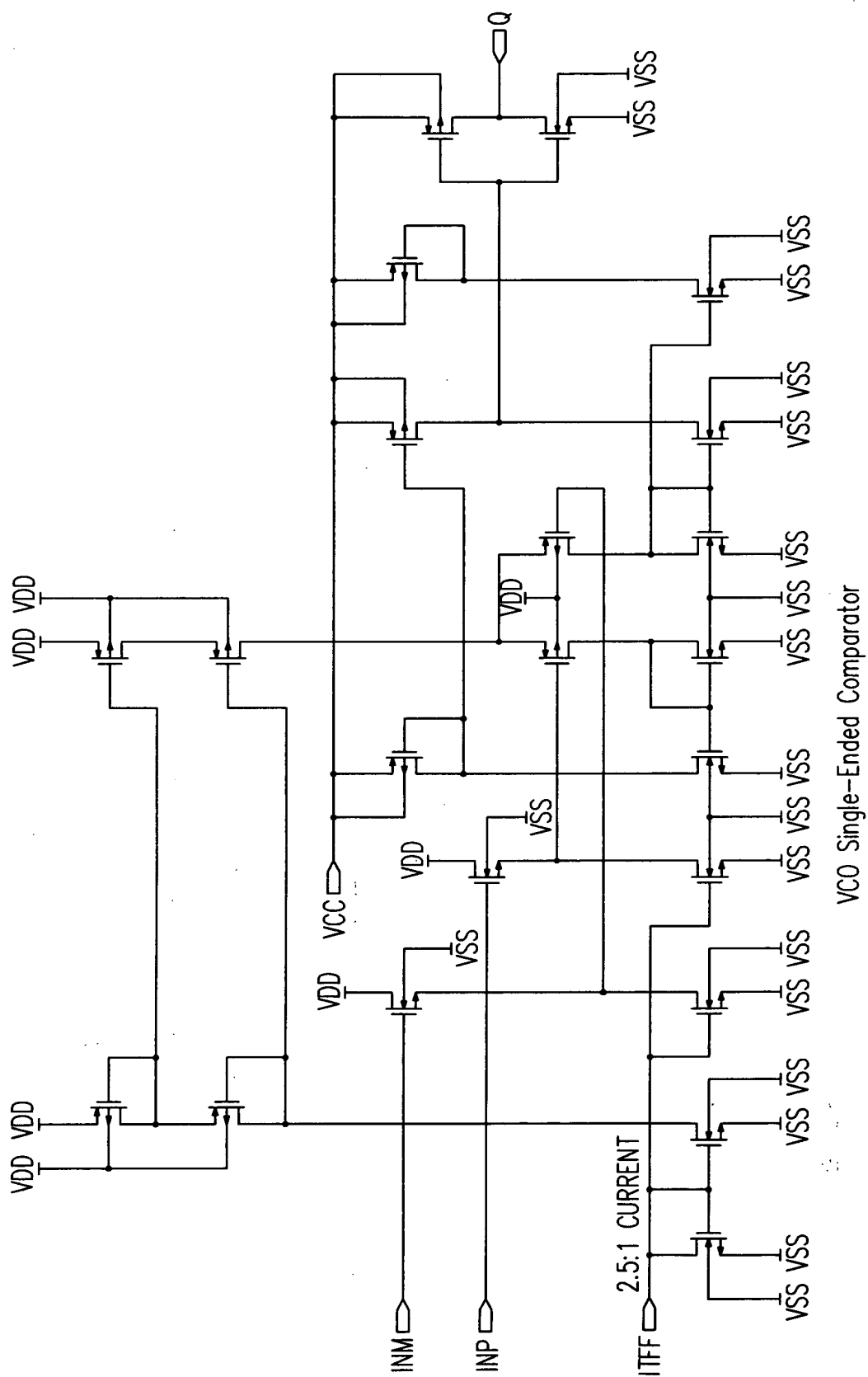
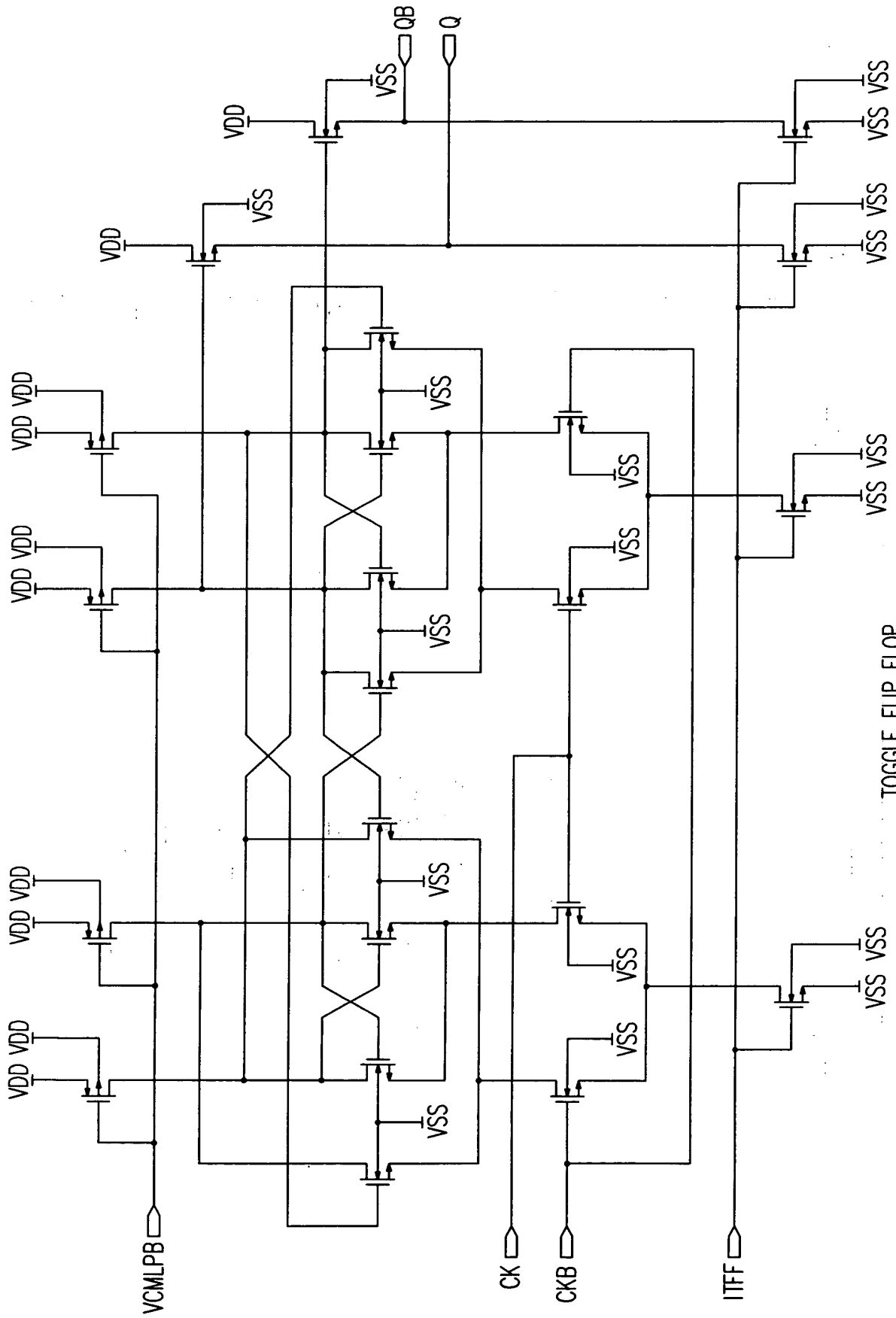


FIG. 43



TOGGLE FLIP FLOP

FIG. 44

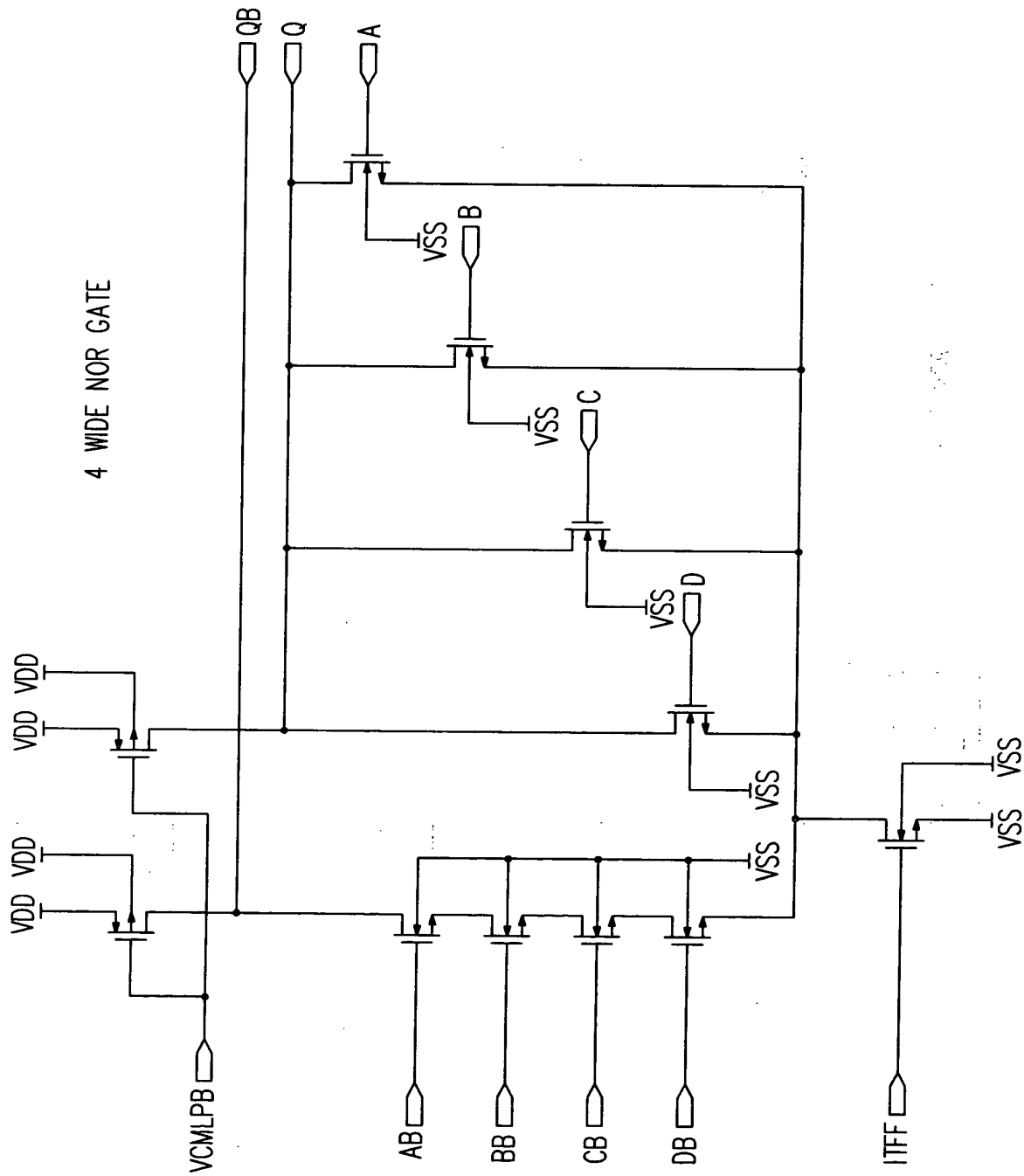


FIG. 45

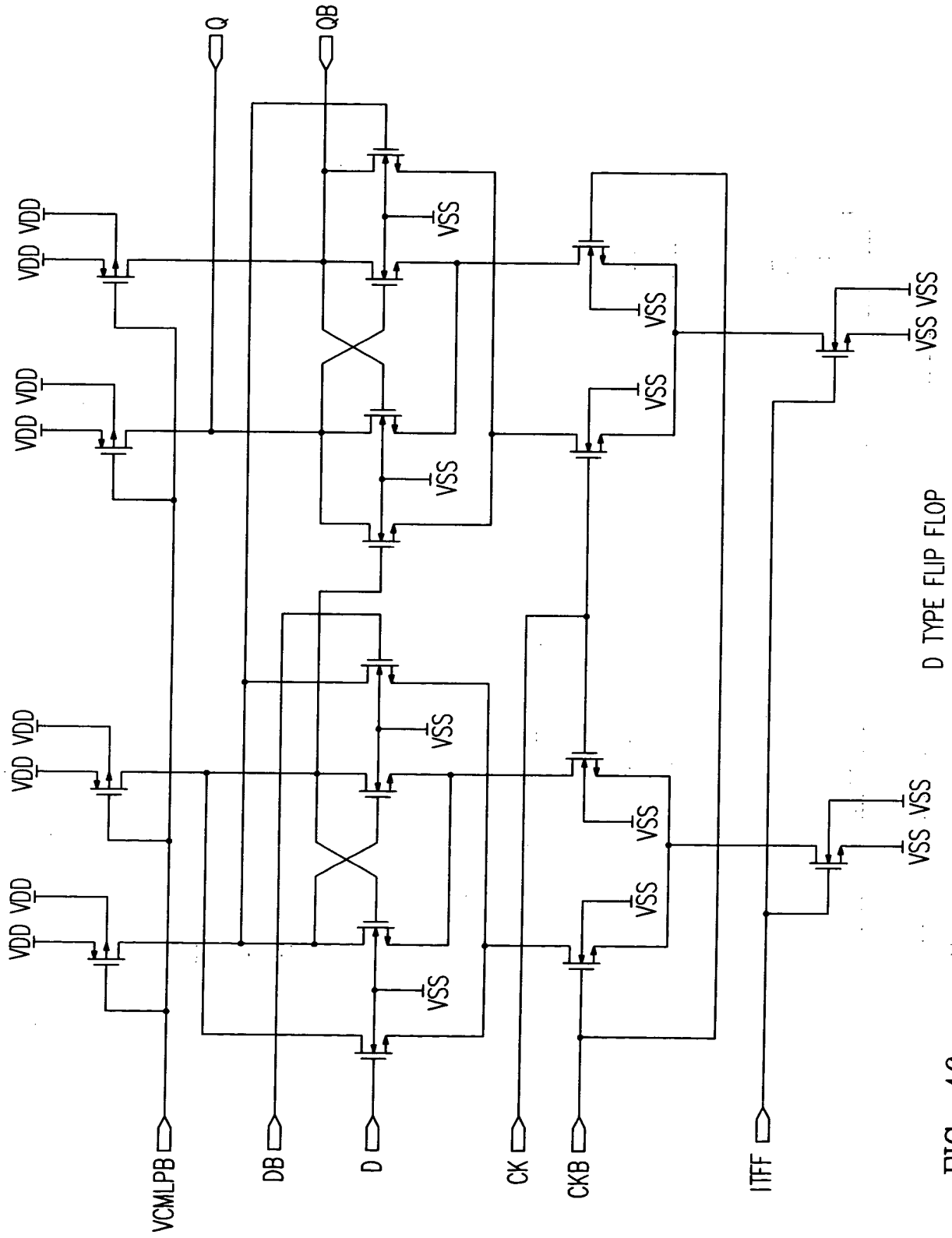


FIG. 46

D TYPE FLIP FLOP

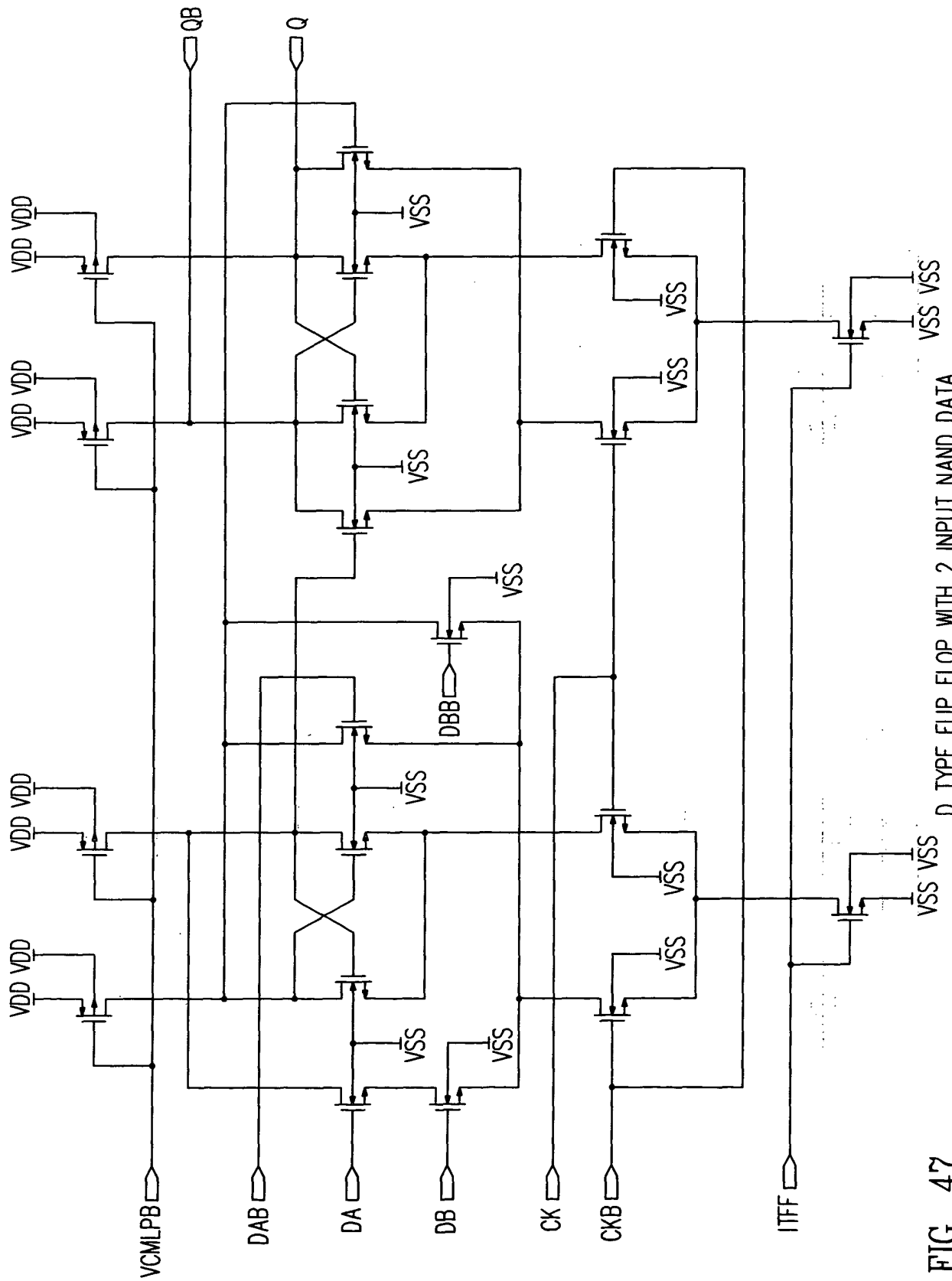


FIG. 47

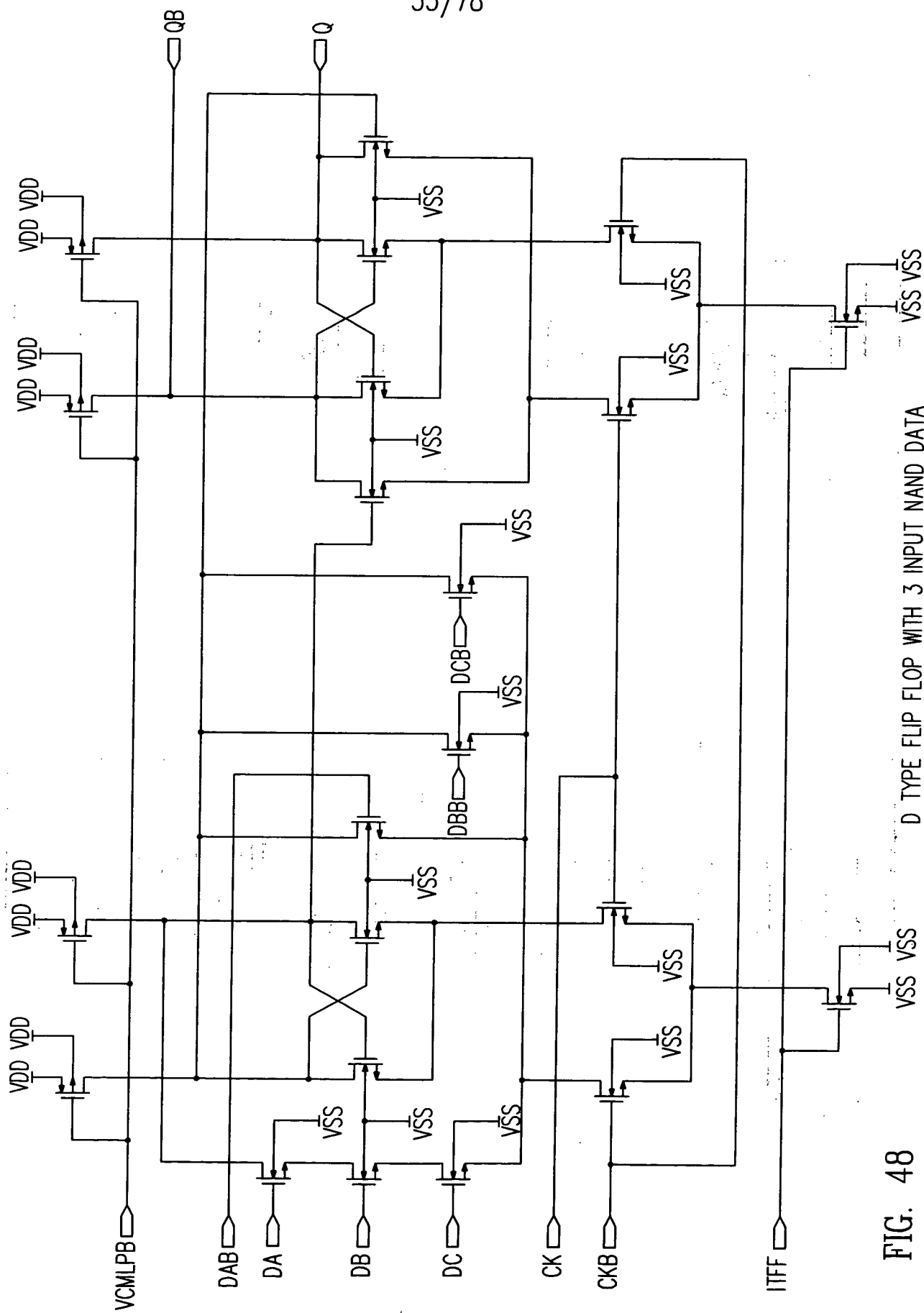
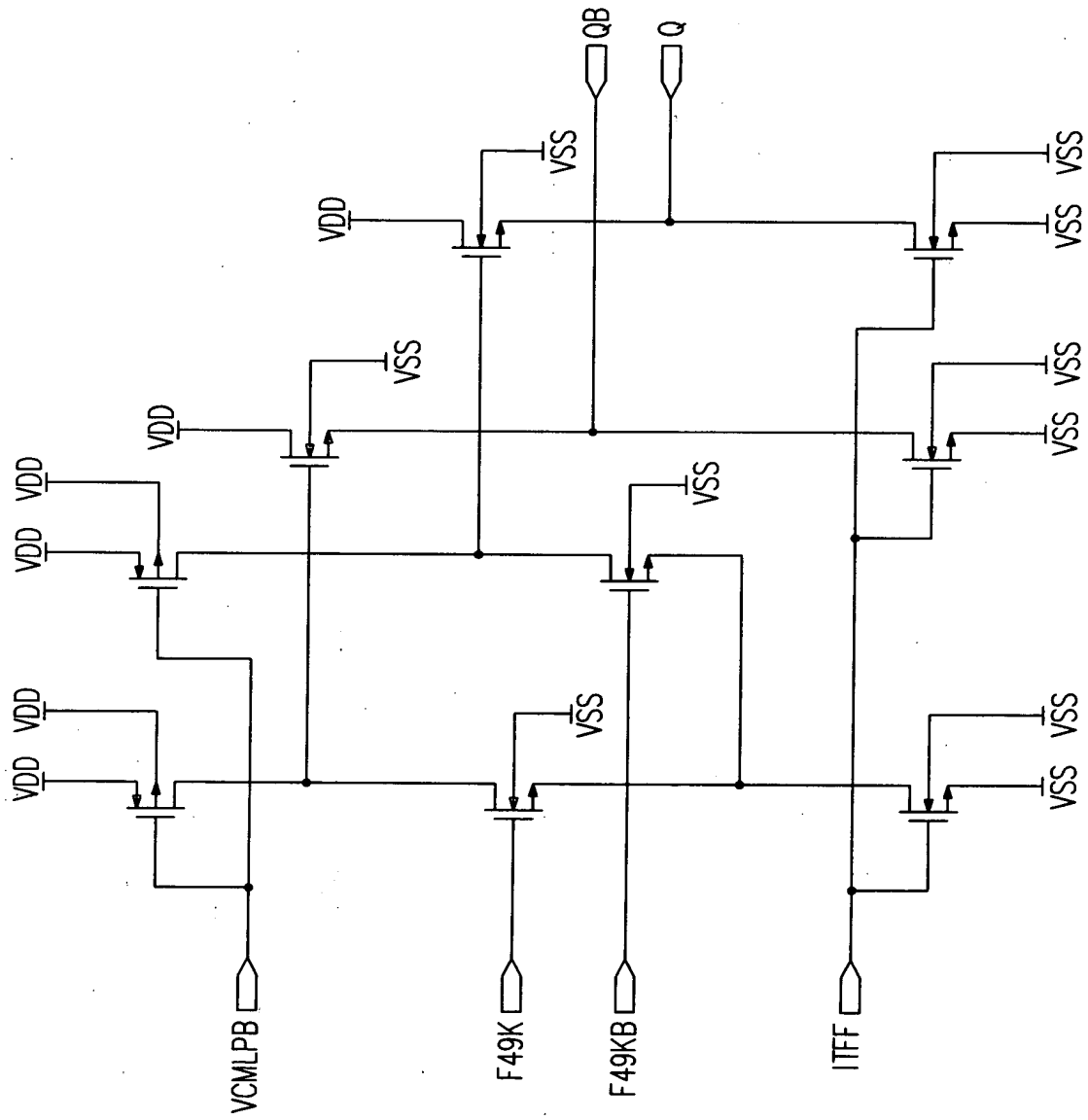


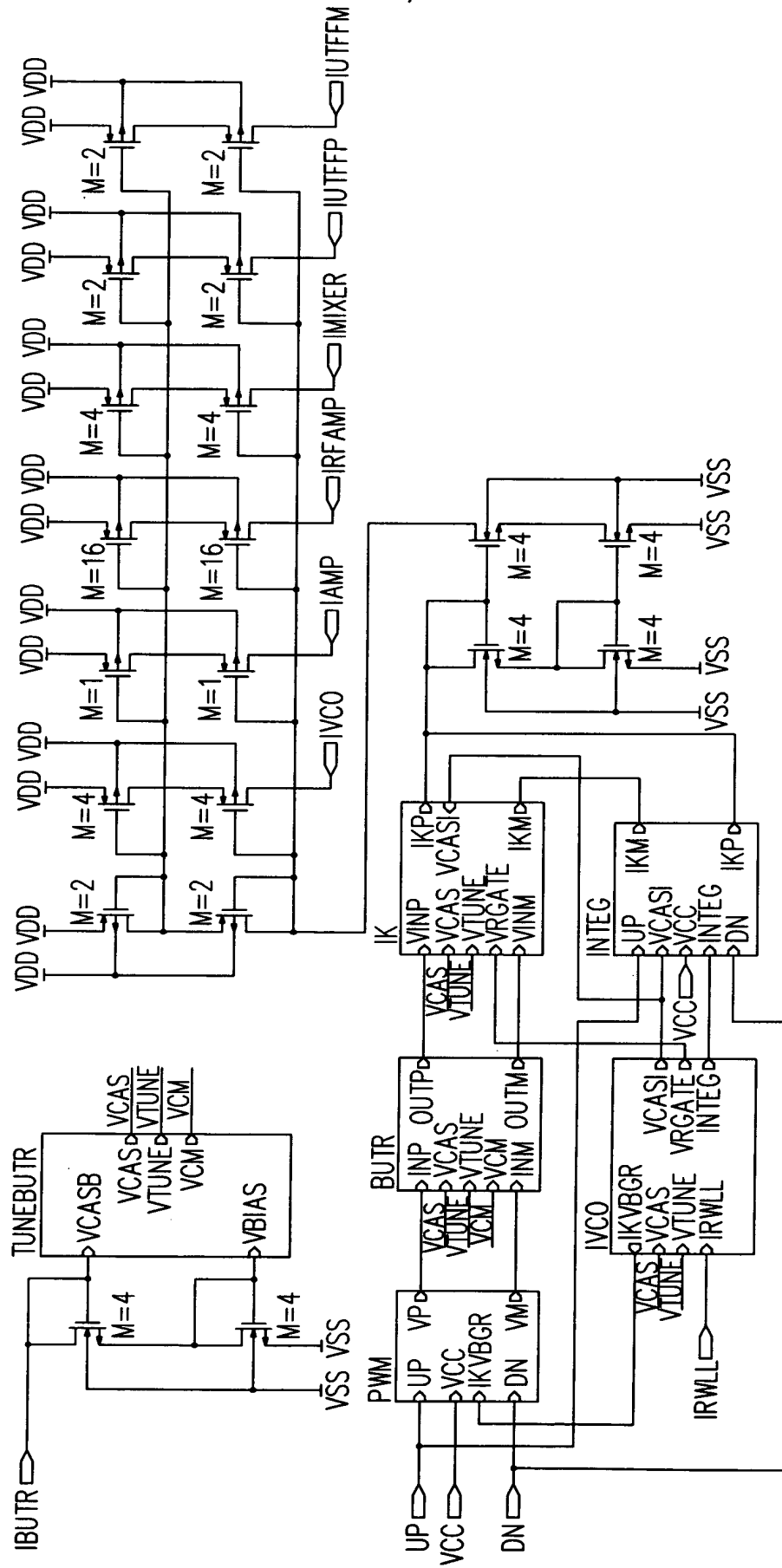
FIG. 48

D TYPE FLIP FLOP WITH 3 INPUT NAND DATA



64/65 PRESCALER LEVEL SHIFTER

FIG. 49



VCO LAG-LEAD INTEGRATOR

FIG. 50

Tuning Bias Generator For Butterworth Bandpass Filter

Note: Note the use of 3X device scalings

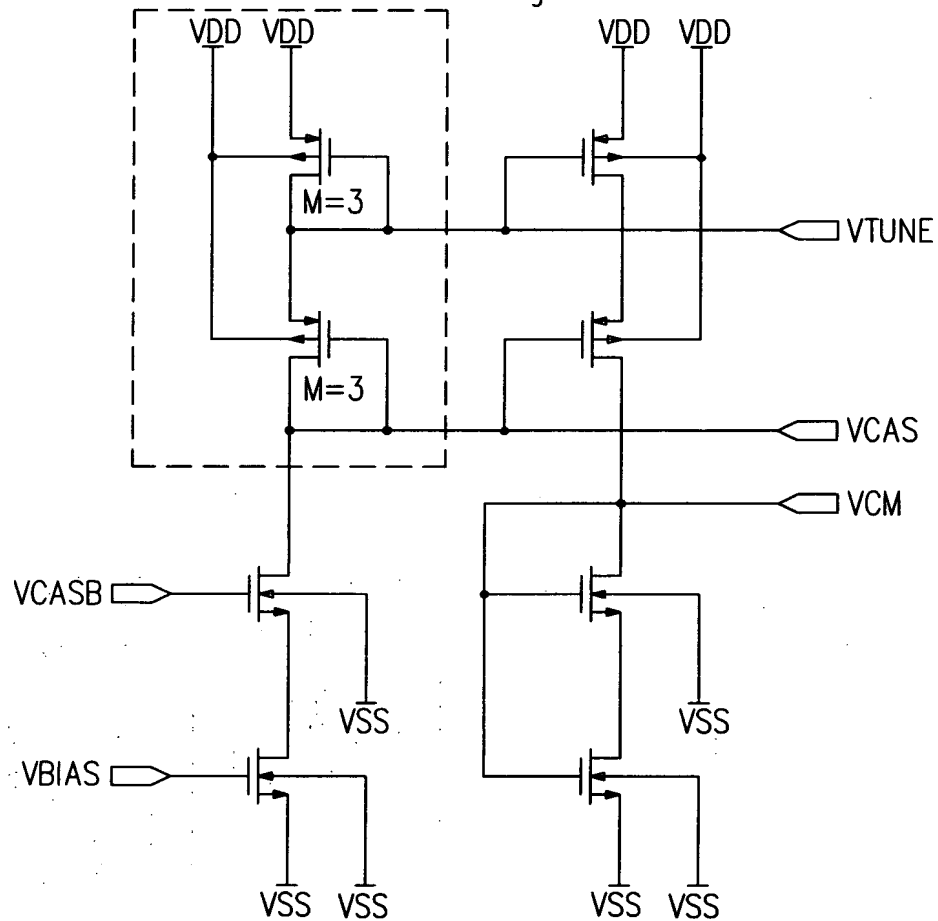


FIG. 51

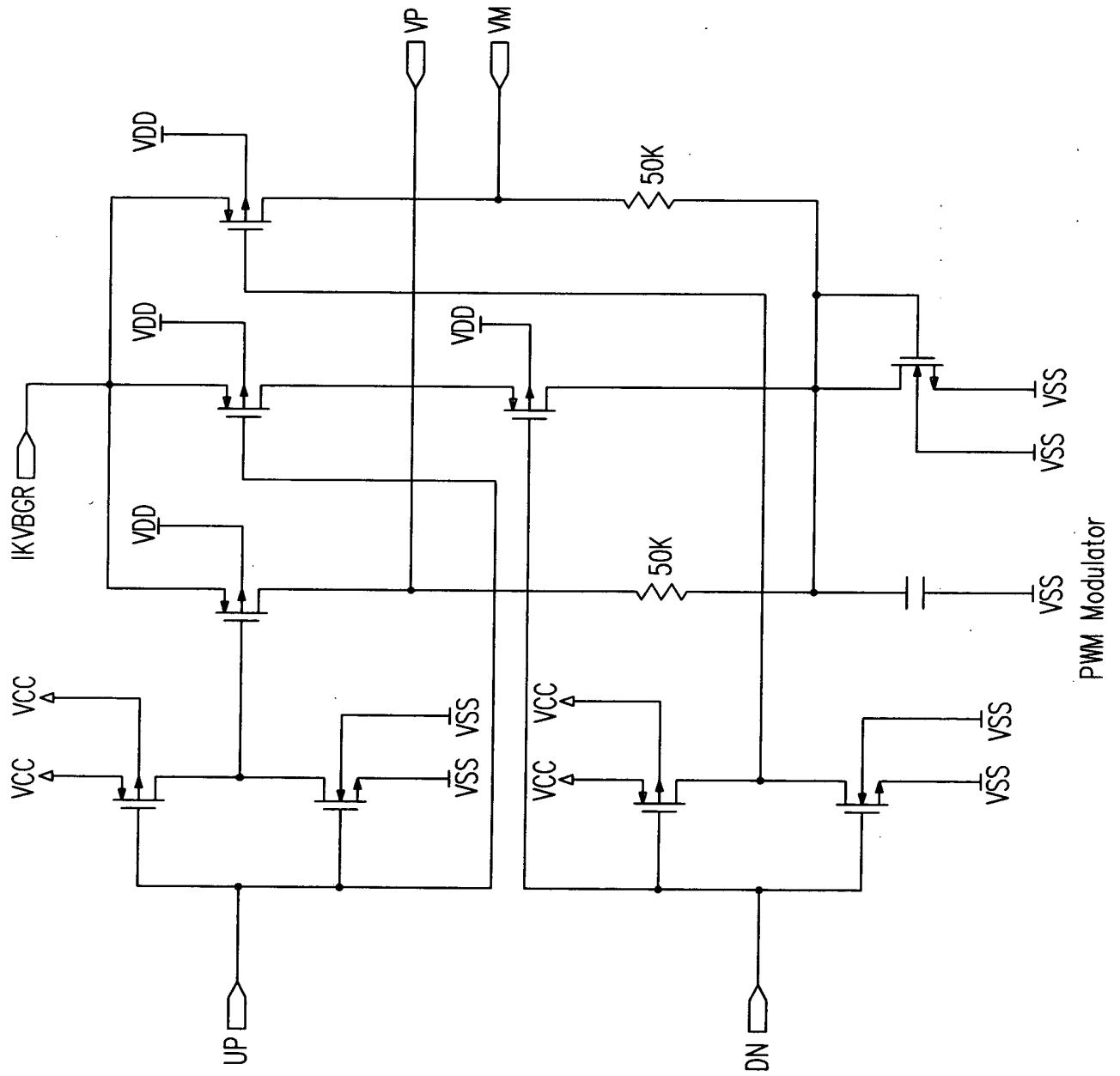
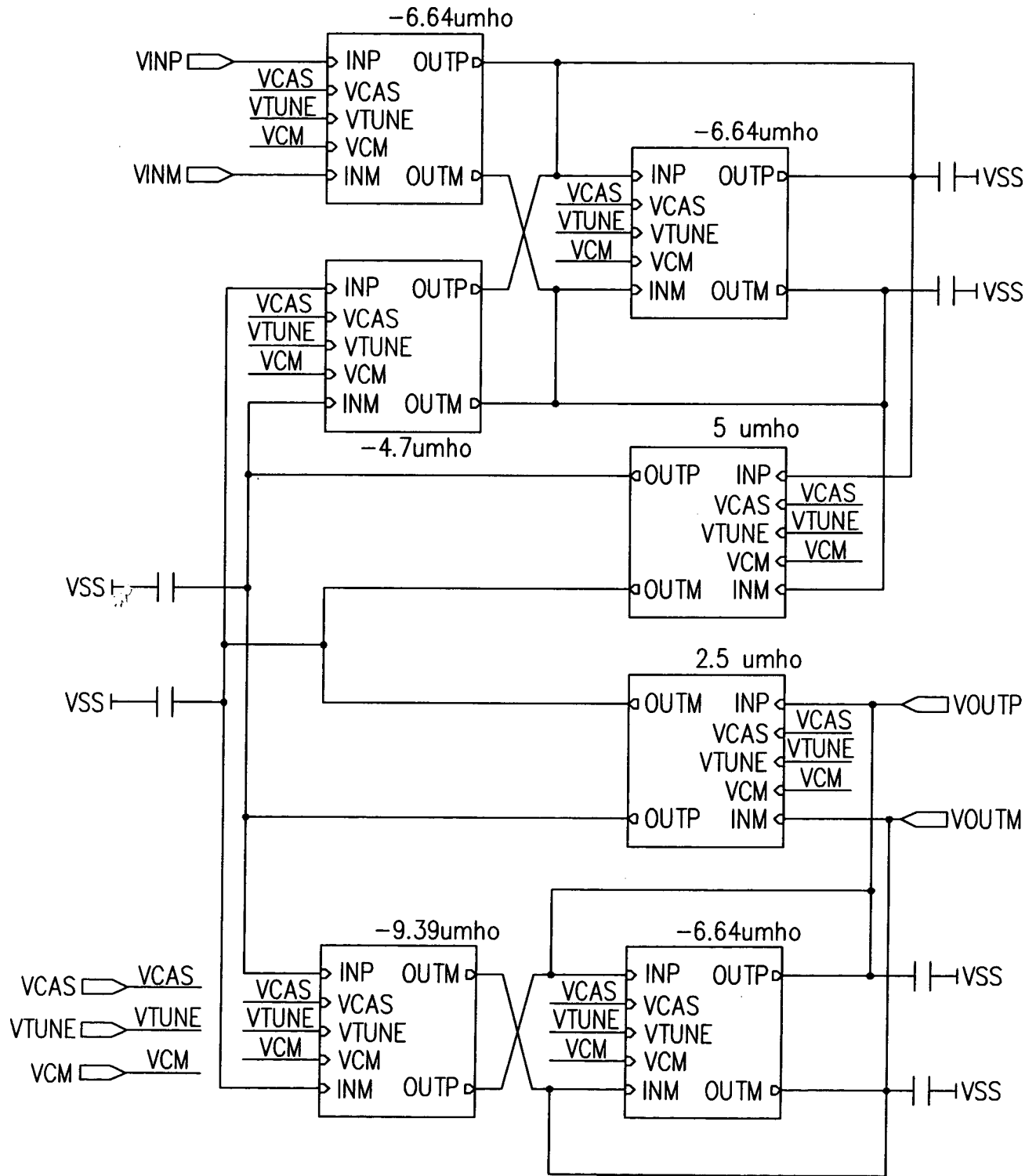


FIG. 52



Butterworth 3rd Order Low Pass GM-C Filter
 $f_c = 200\text{KHz}$

FIG. 53

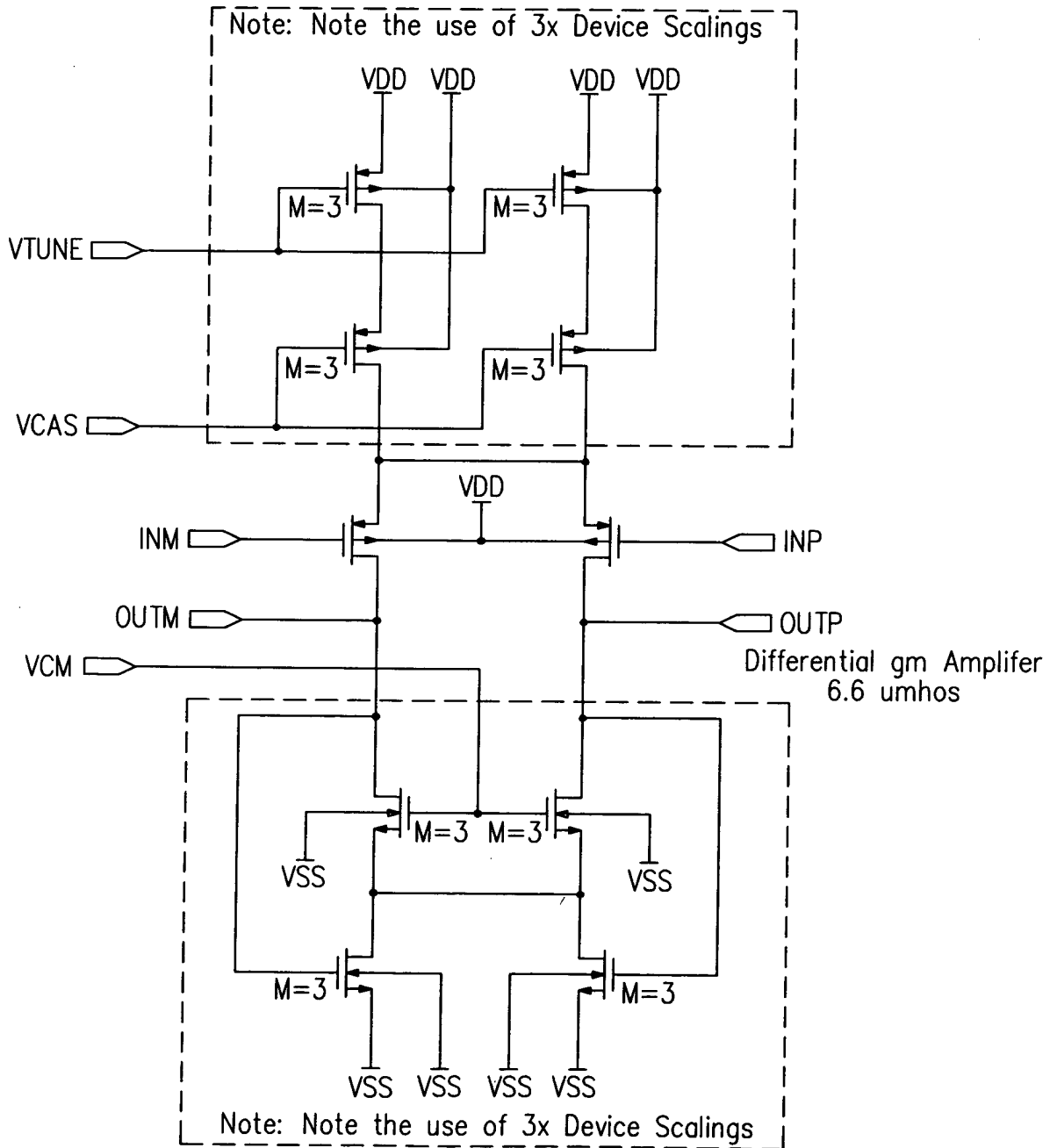


FIG. 54

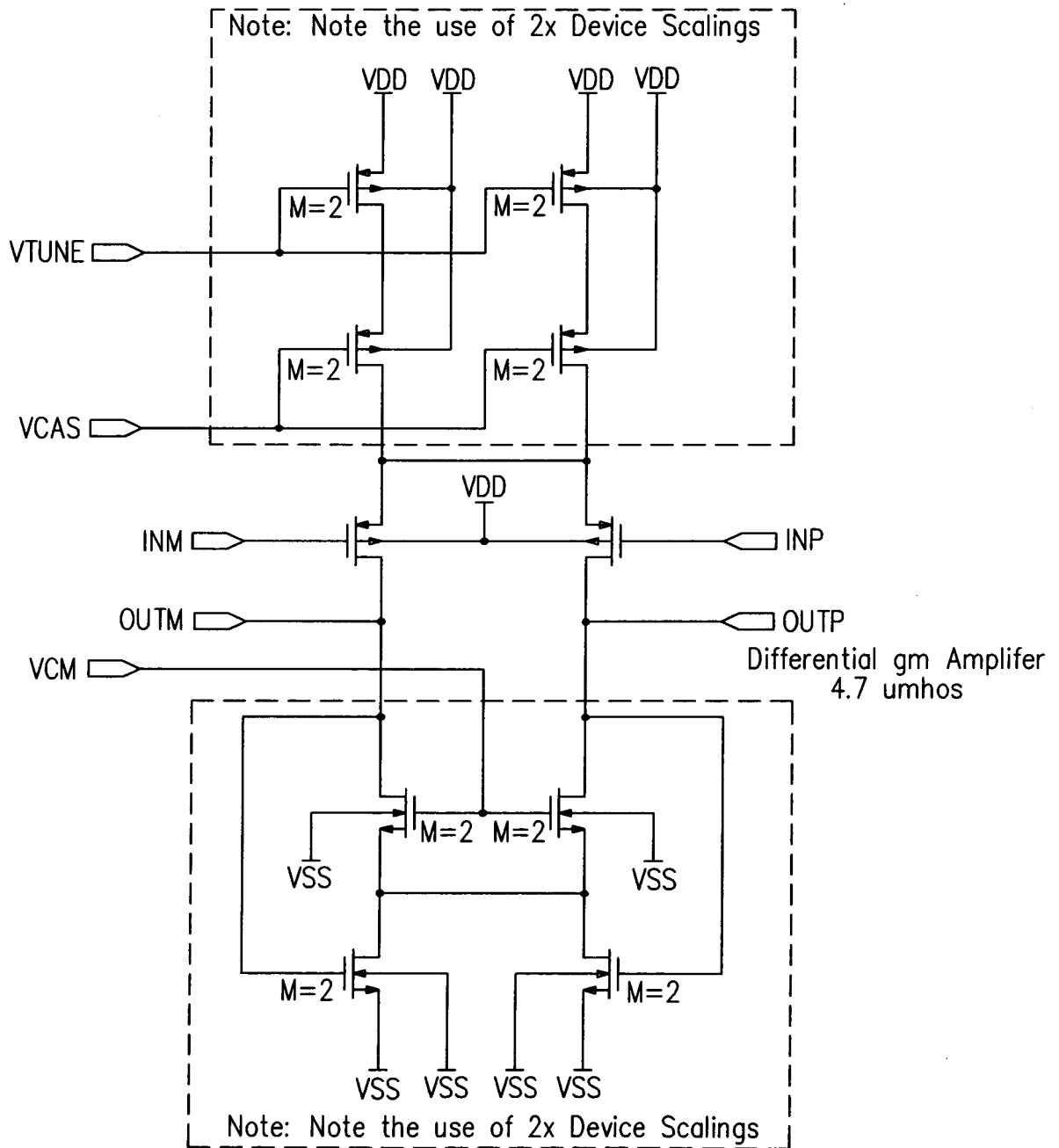


FIG. 55

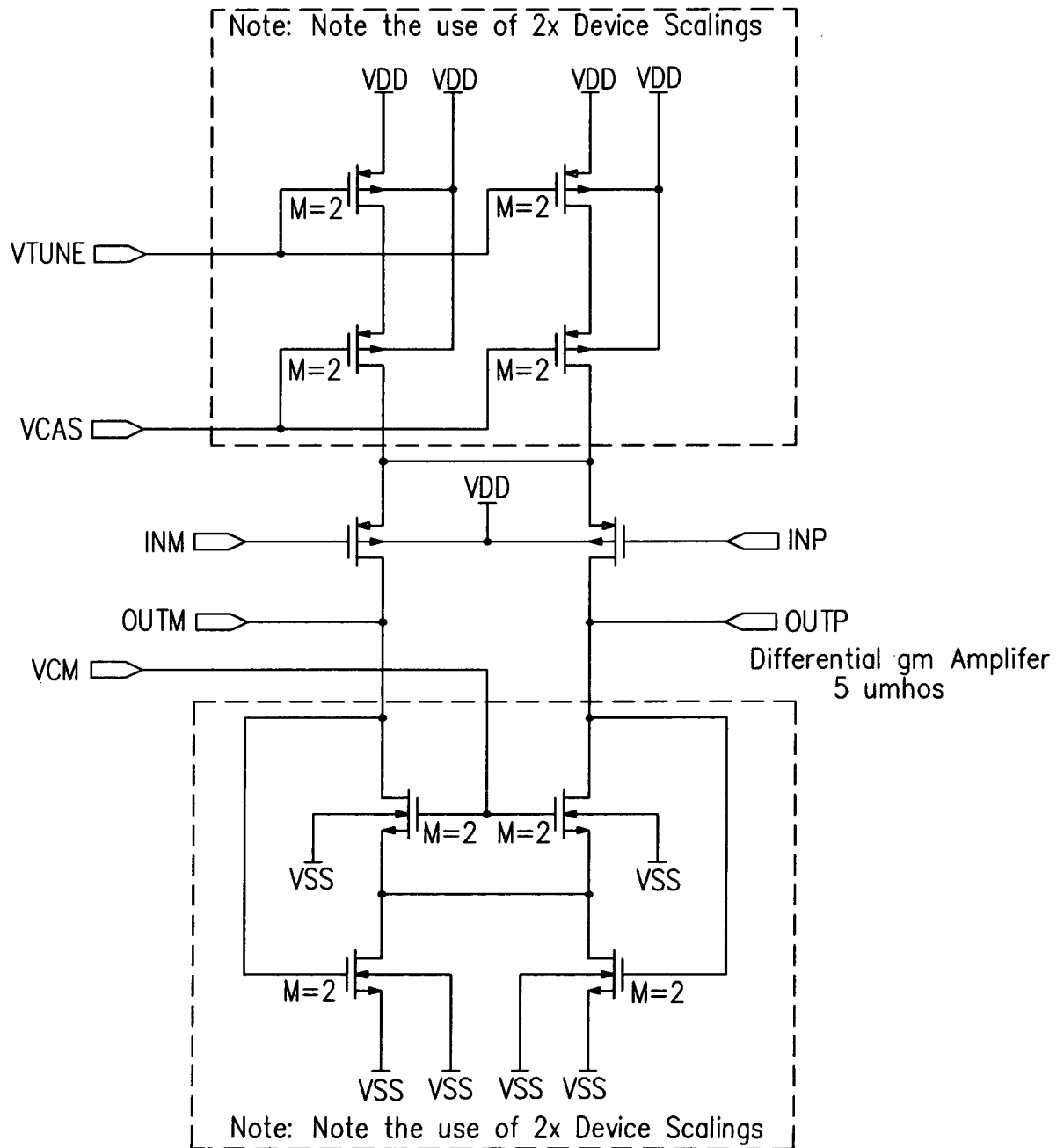


FIG. 56



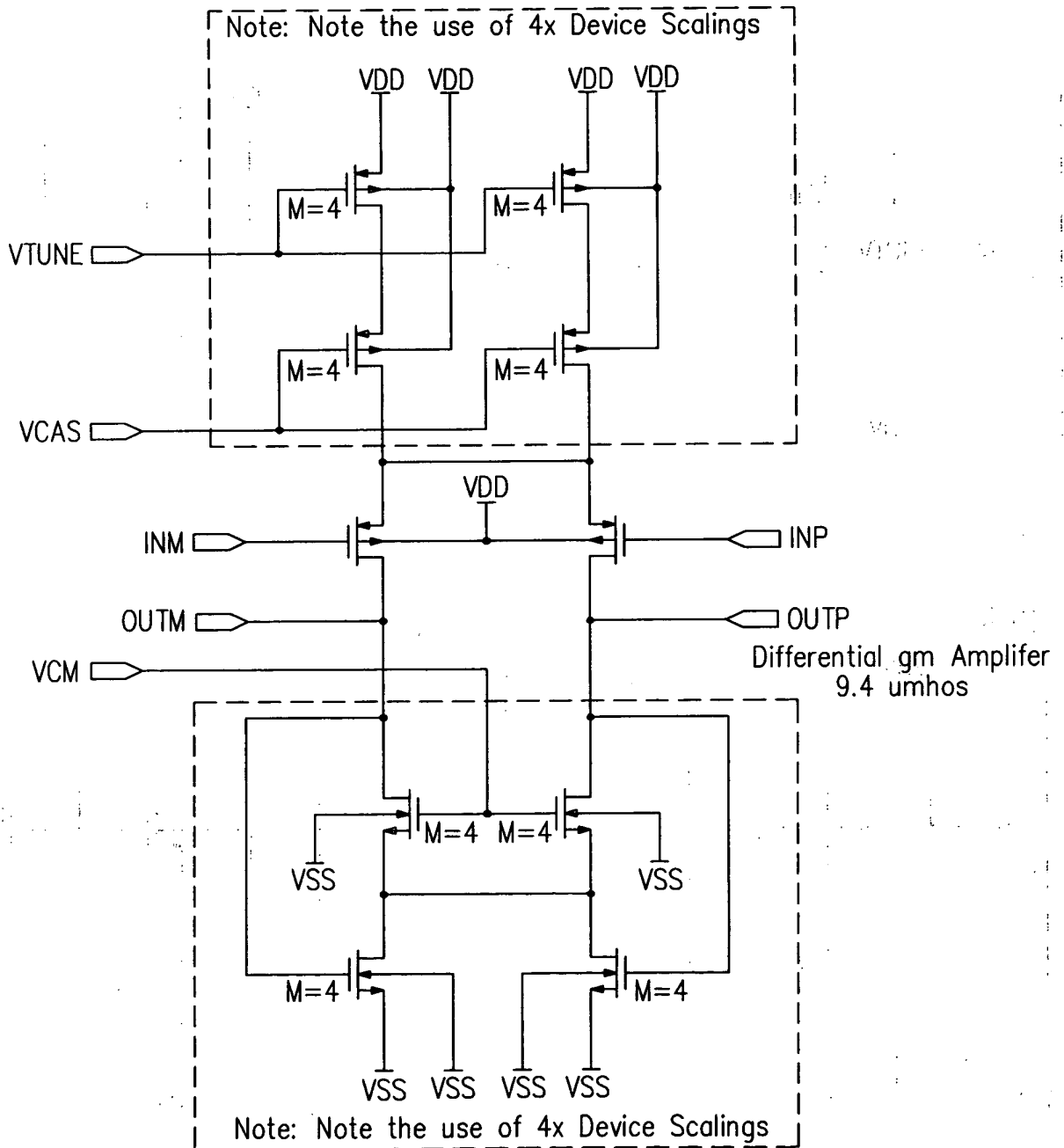


FIG. 58

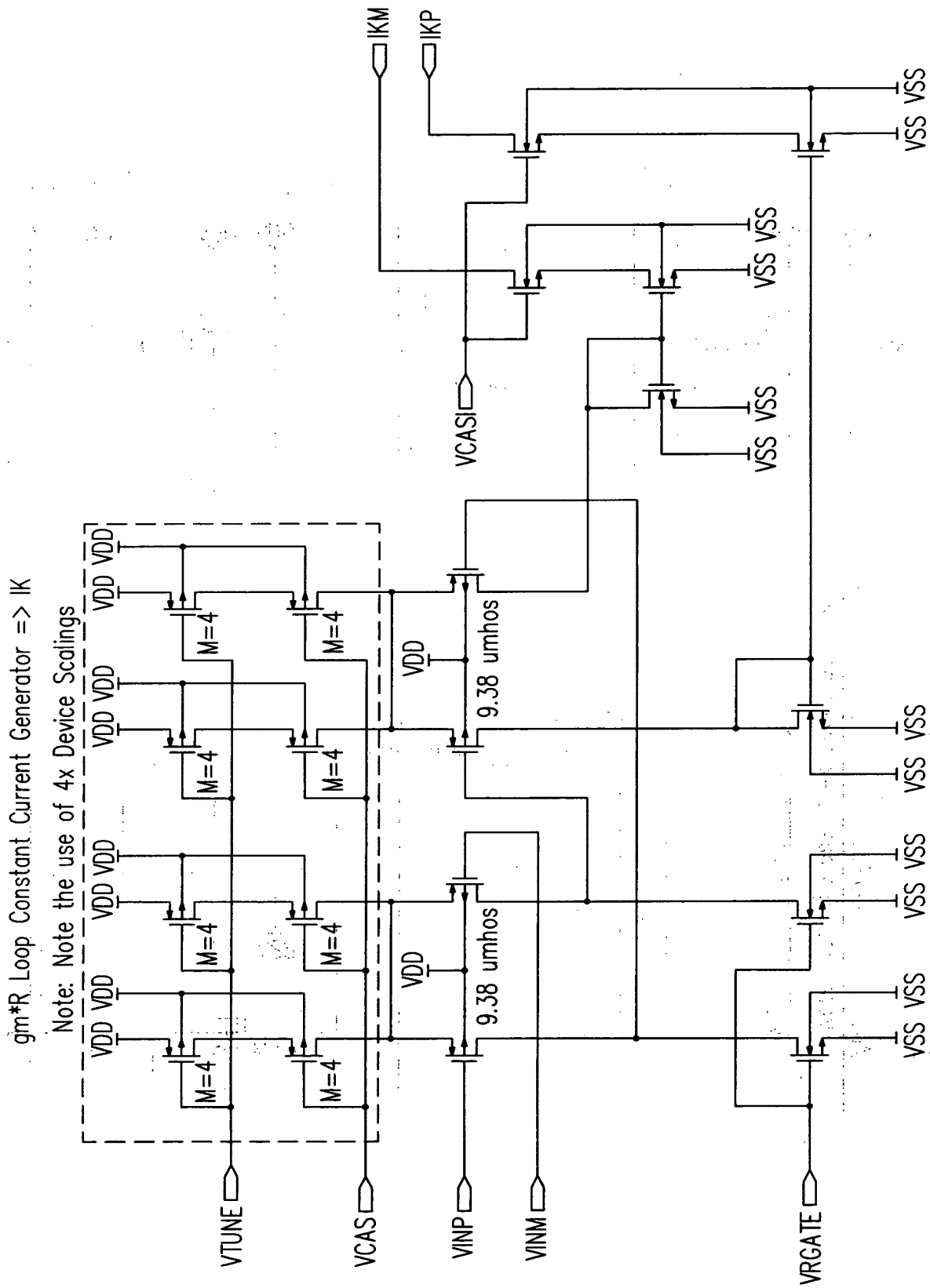


FIG. 59

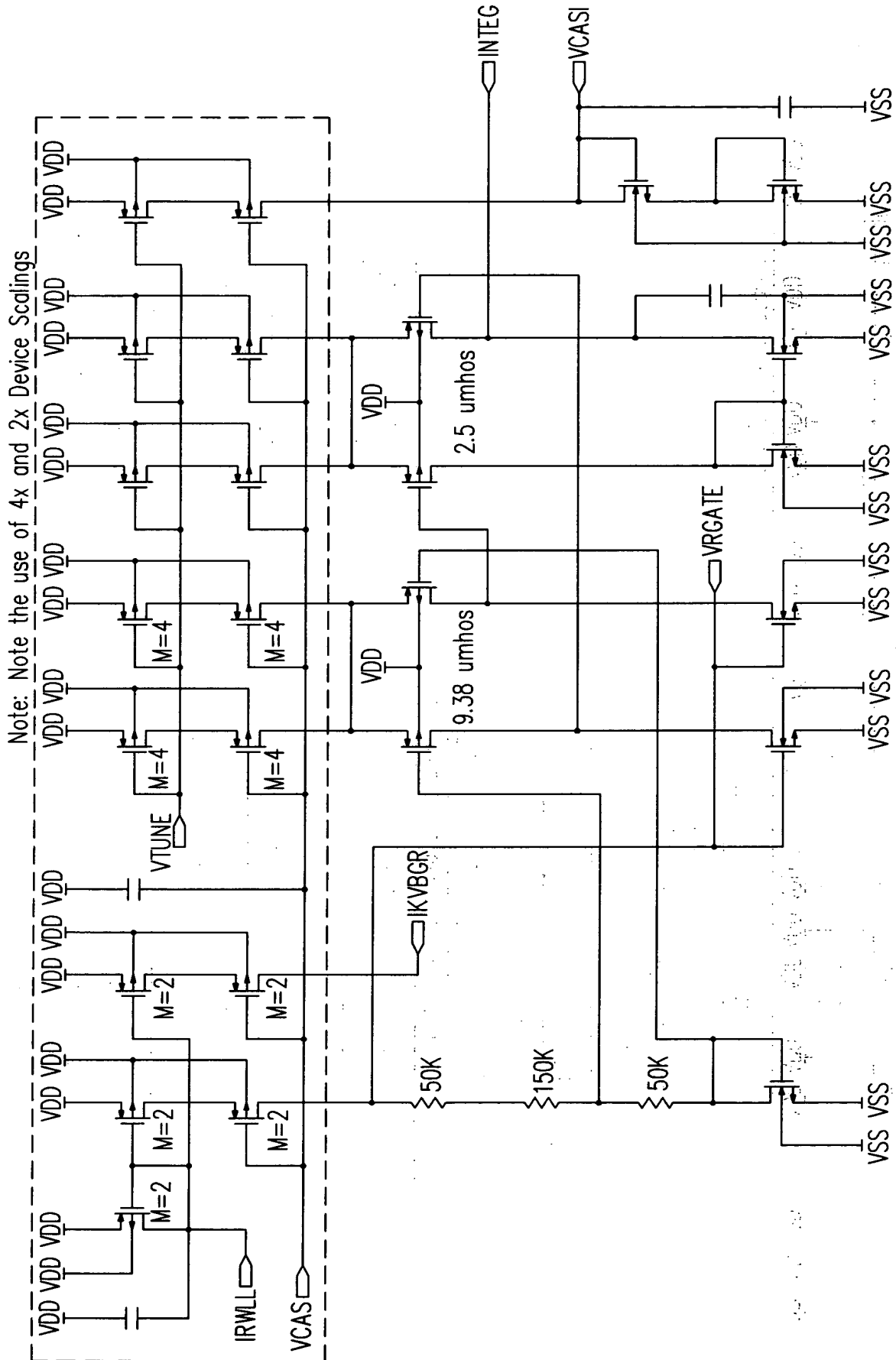
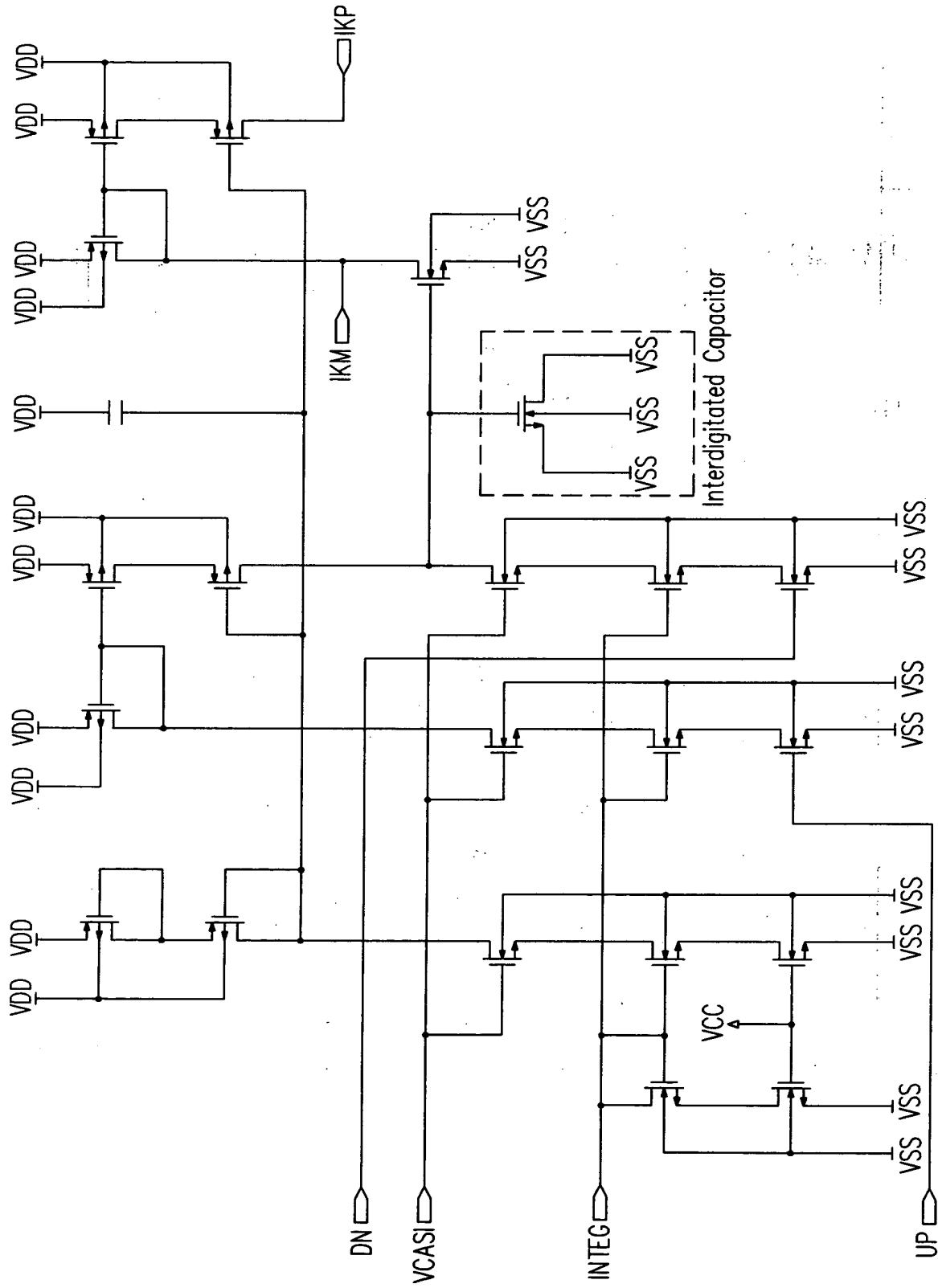


FIG. 60



Sweeping VCO Tuning Integrator

FIG. 61

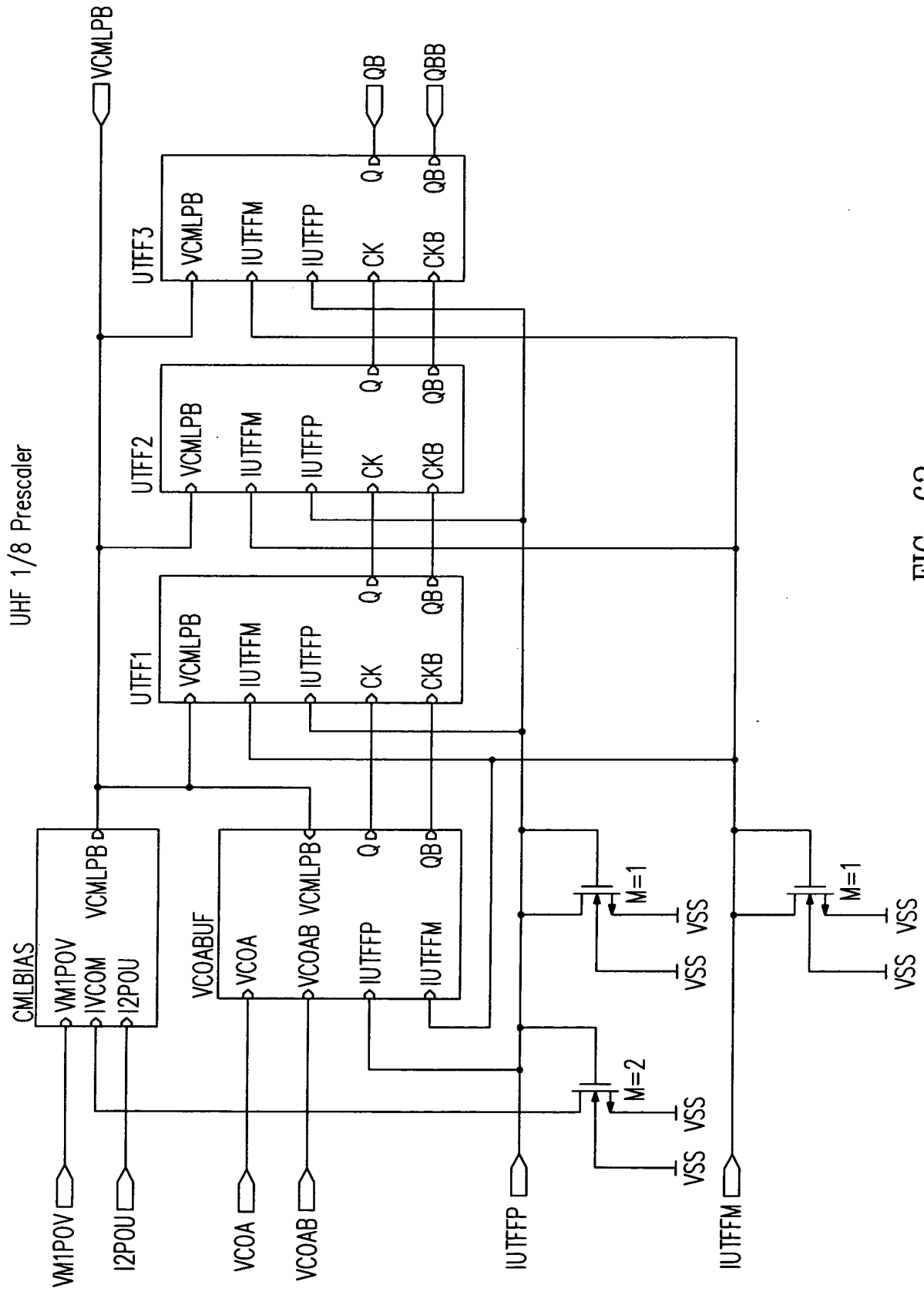
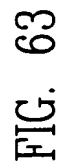


FIG. 62



CML Bias Generator for UHF Divider

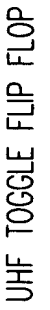


FIG. 64

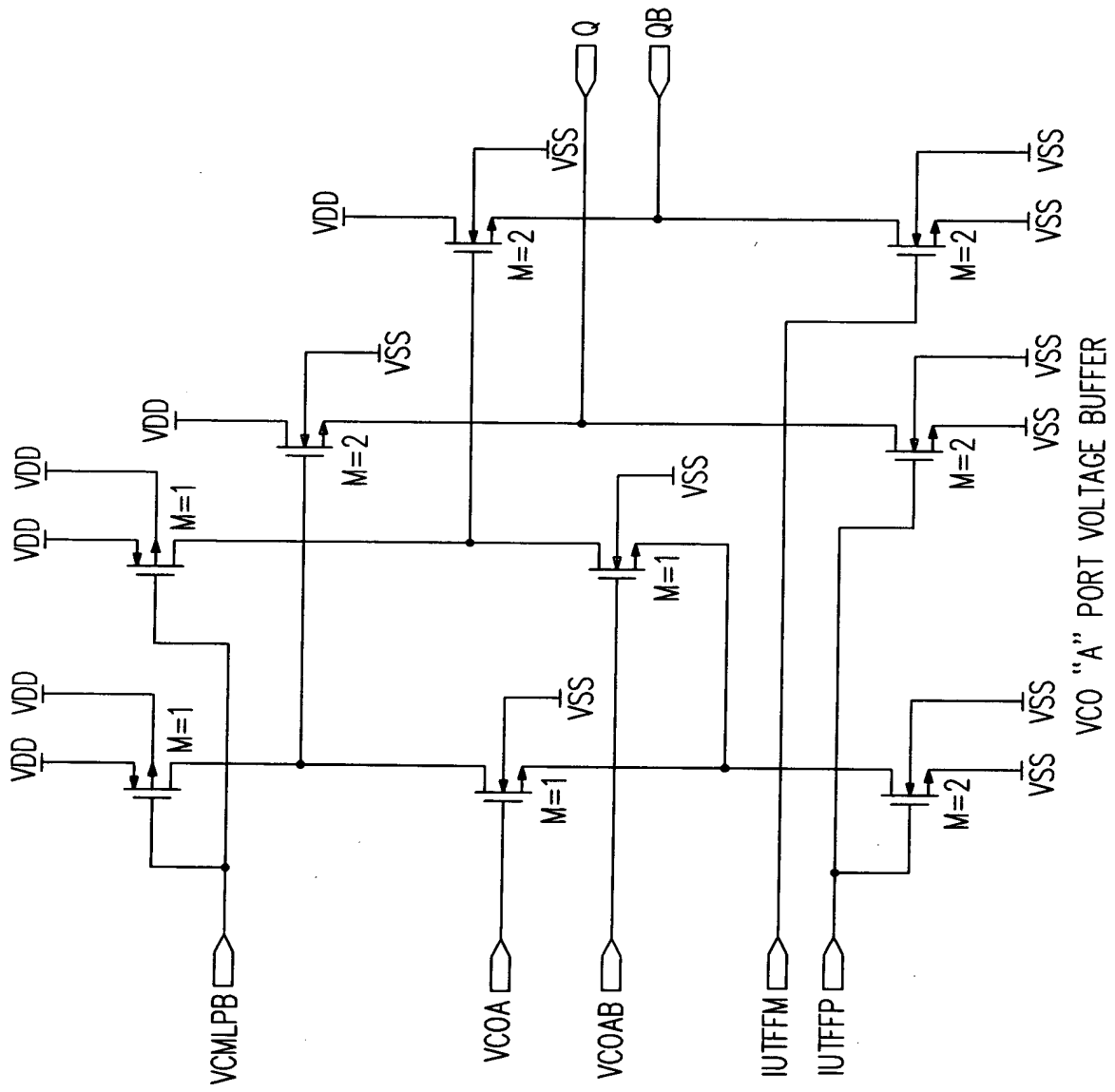


FIG. 65

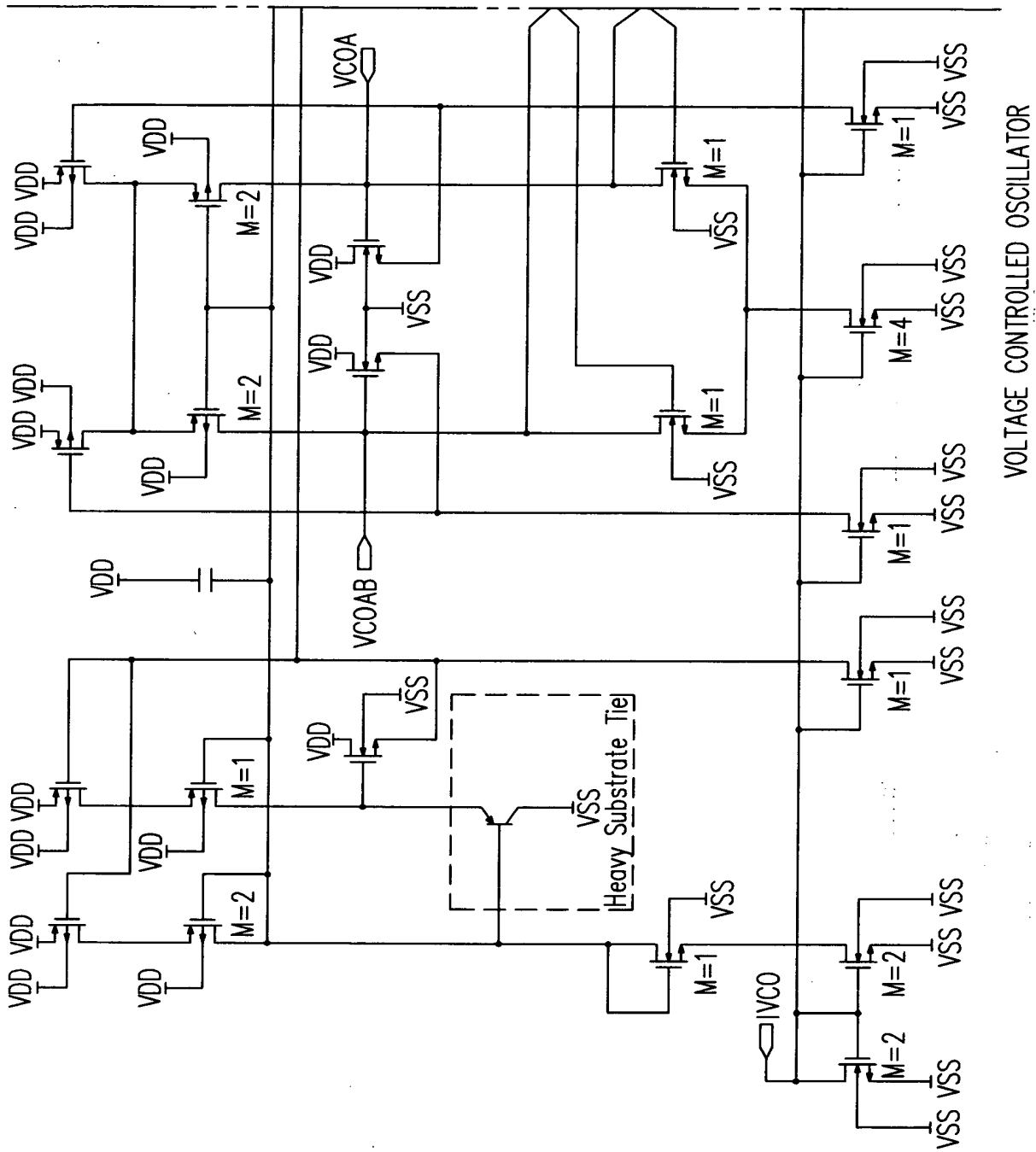
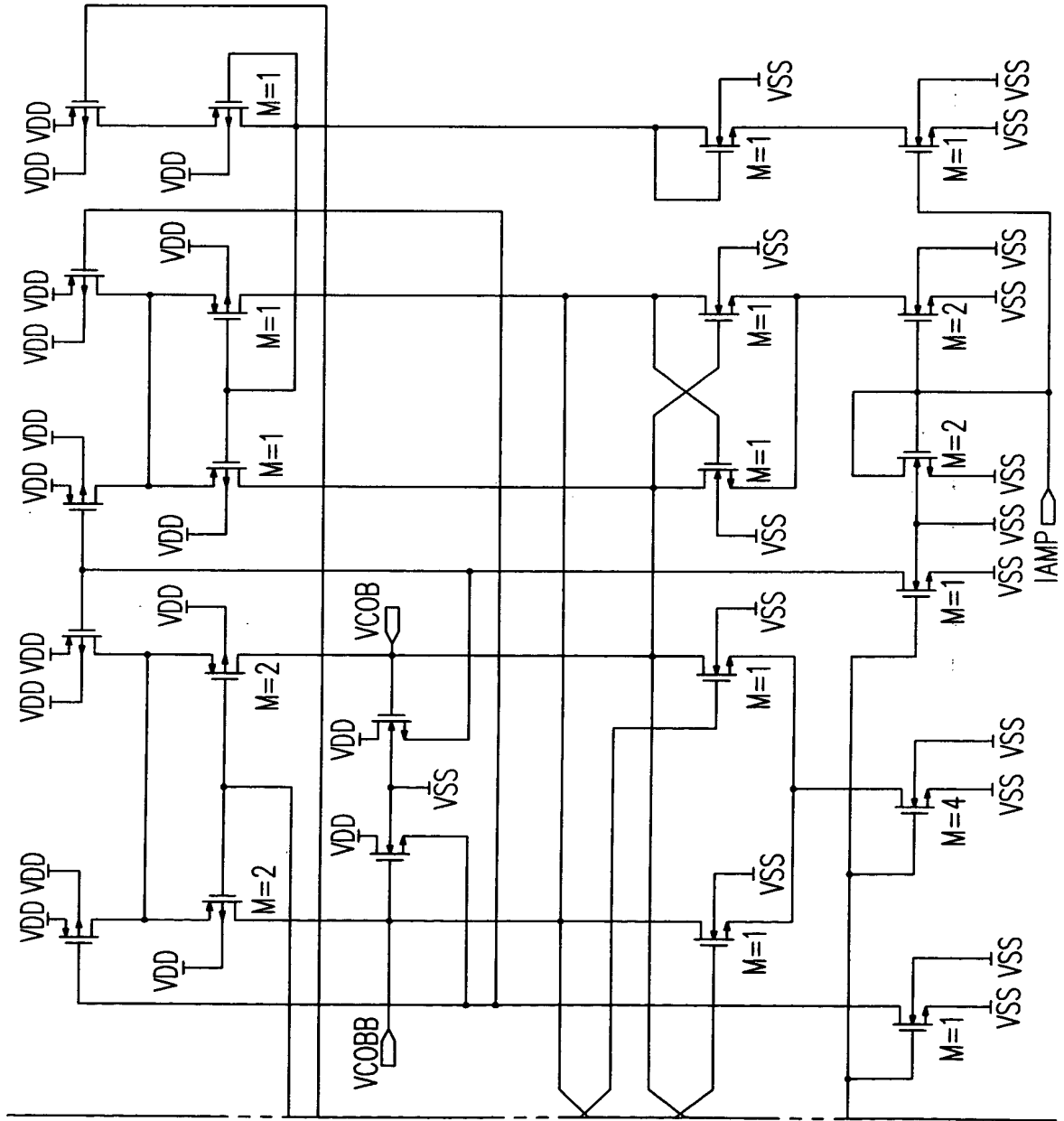


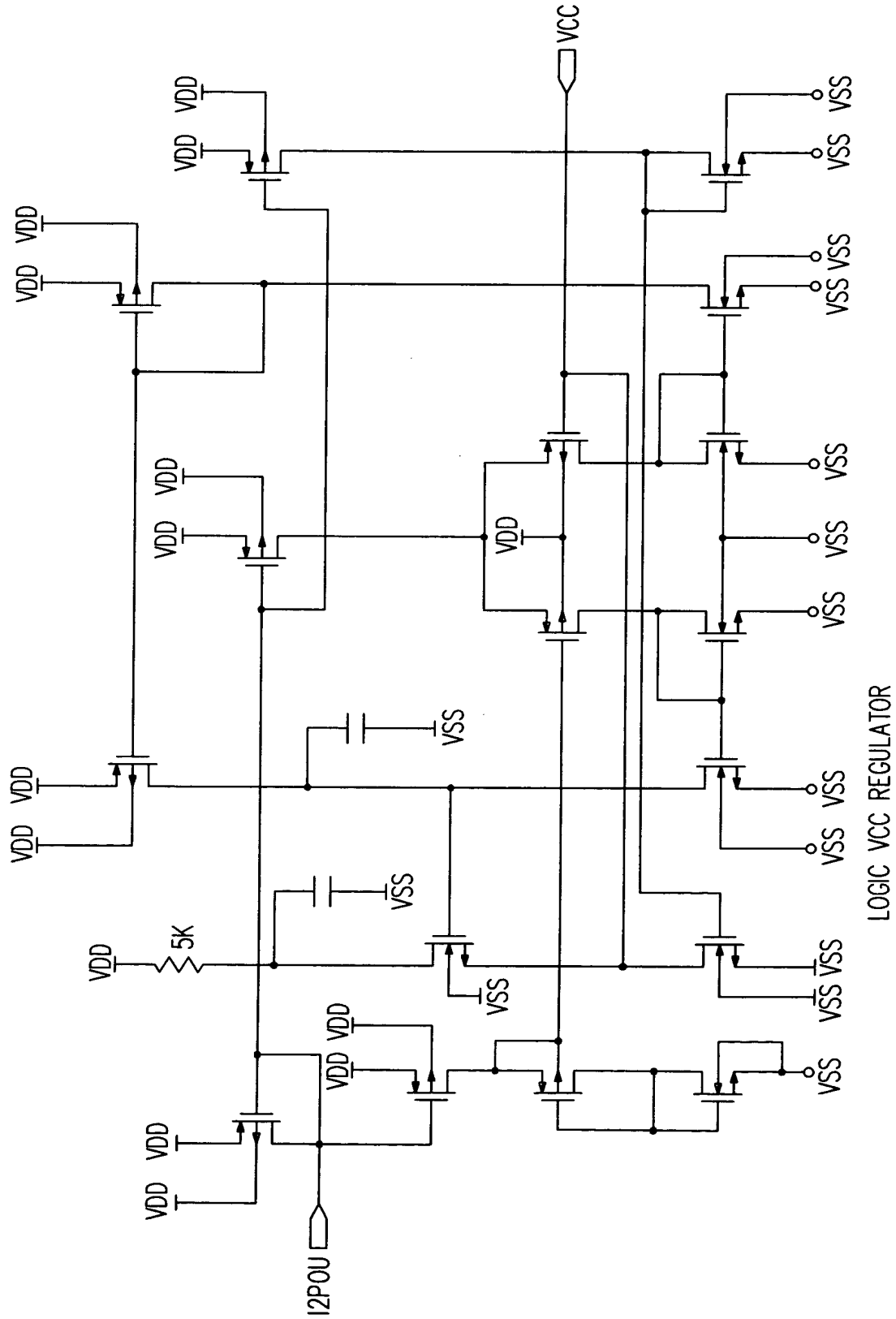
FIG. 66A

FIG. 66A	FIG. 66B
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KEY TO FIG. 66

FIG. 66B





LOGIC VCC REGULATOR

FIG. 67

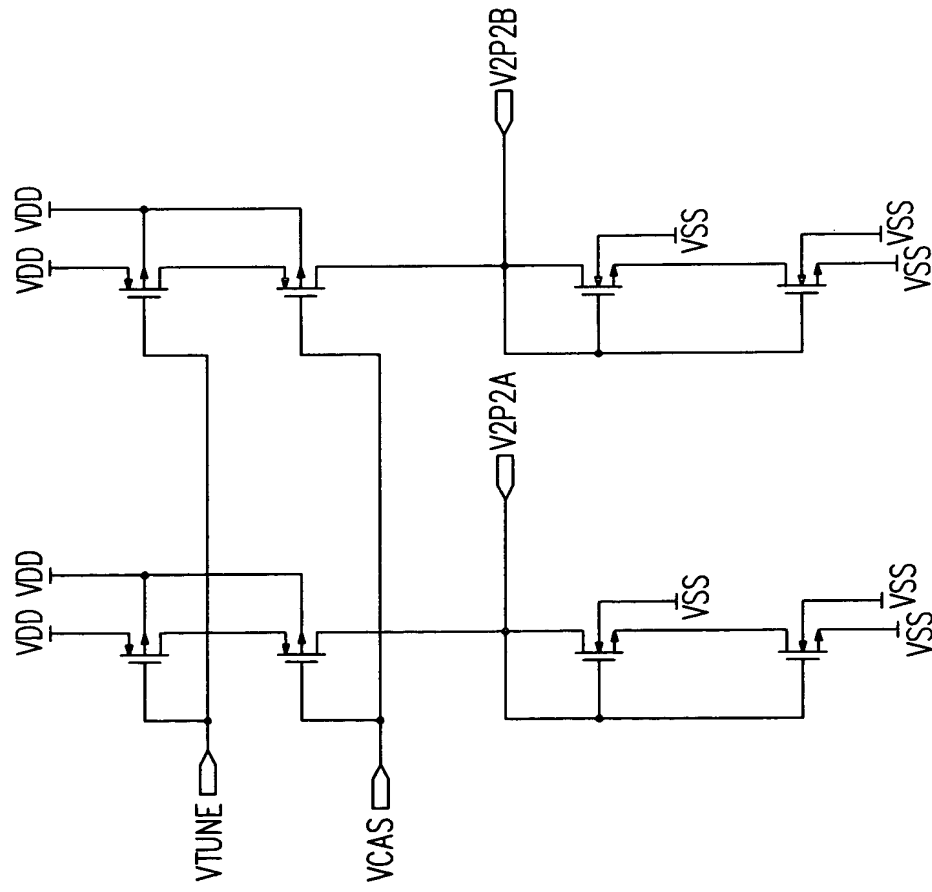


FIG. 68

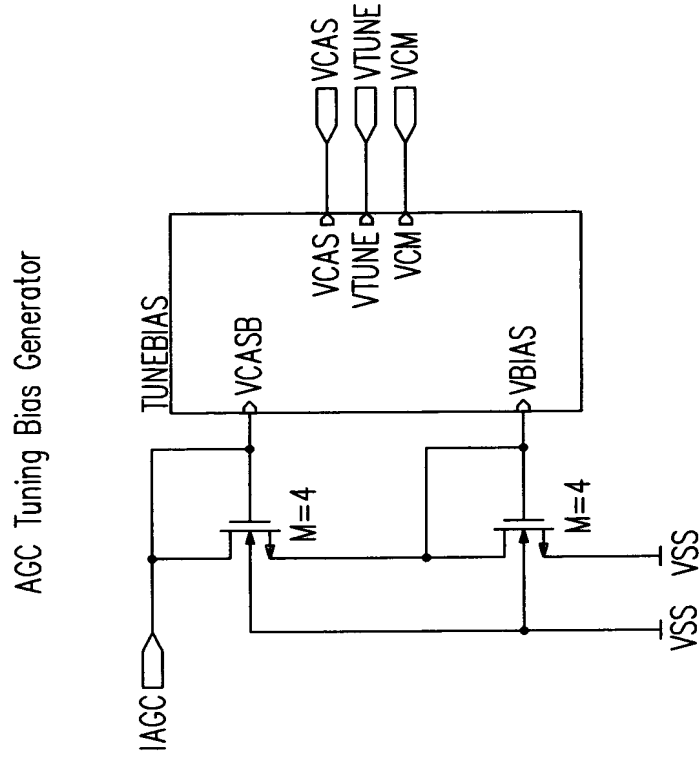
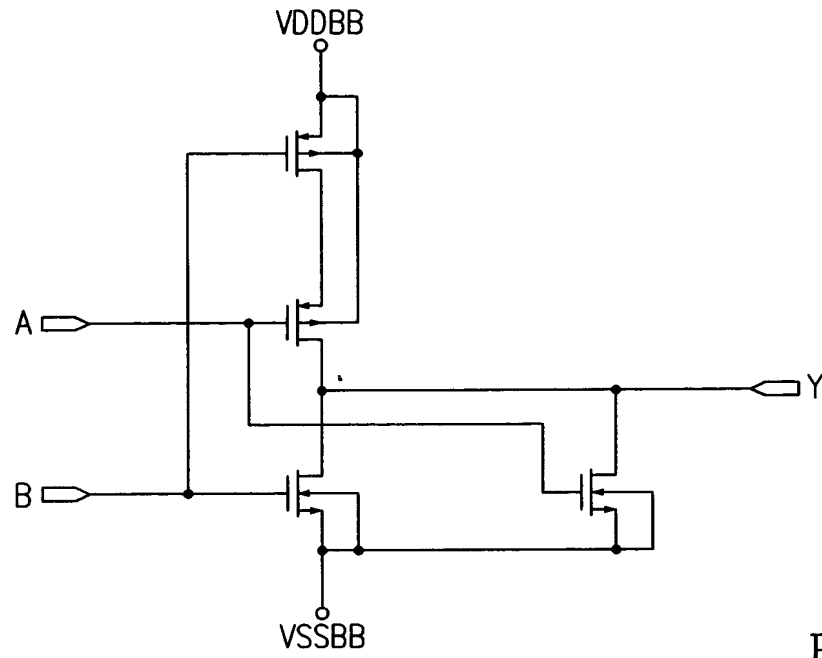
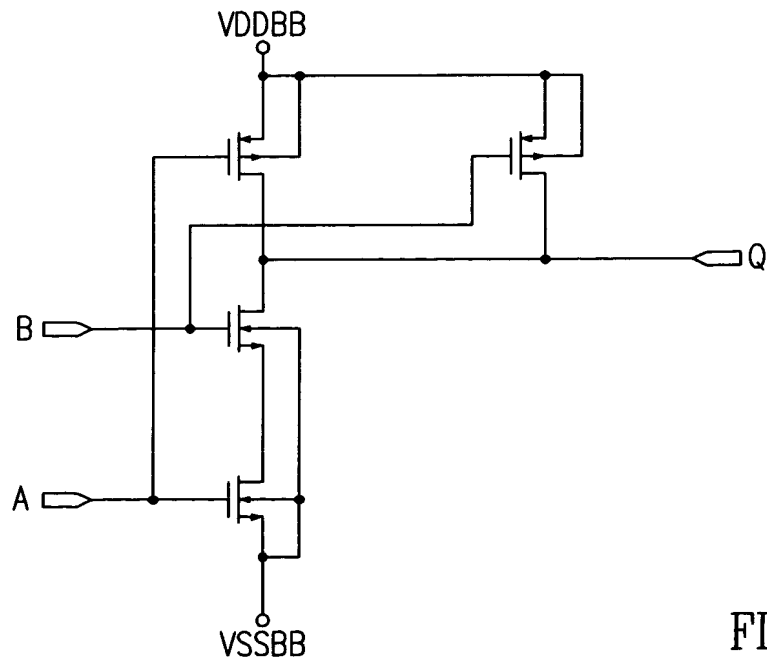


FIG. 69



NOR2

FIG. 70



NAND2

FIG. 71

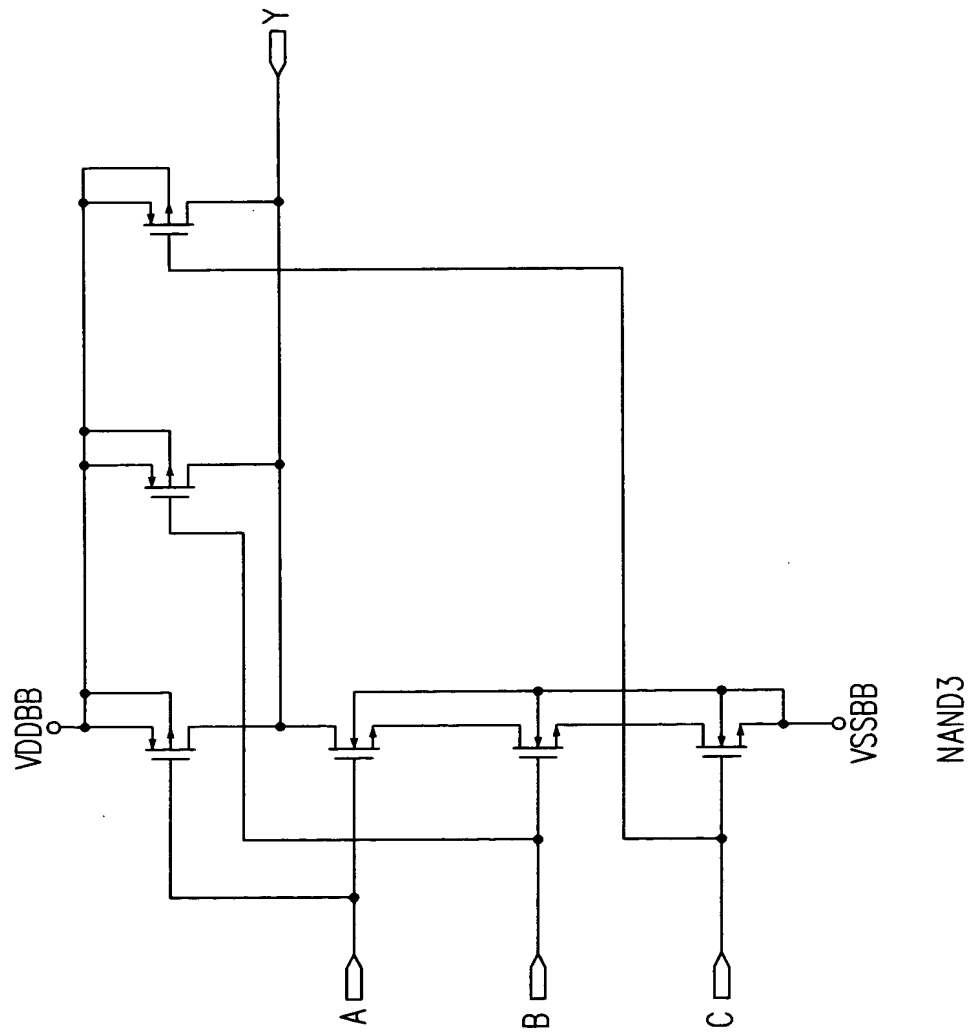


FIG. 72

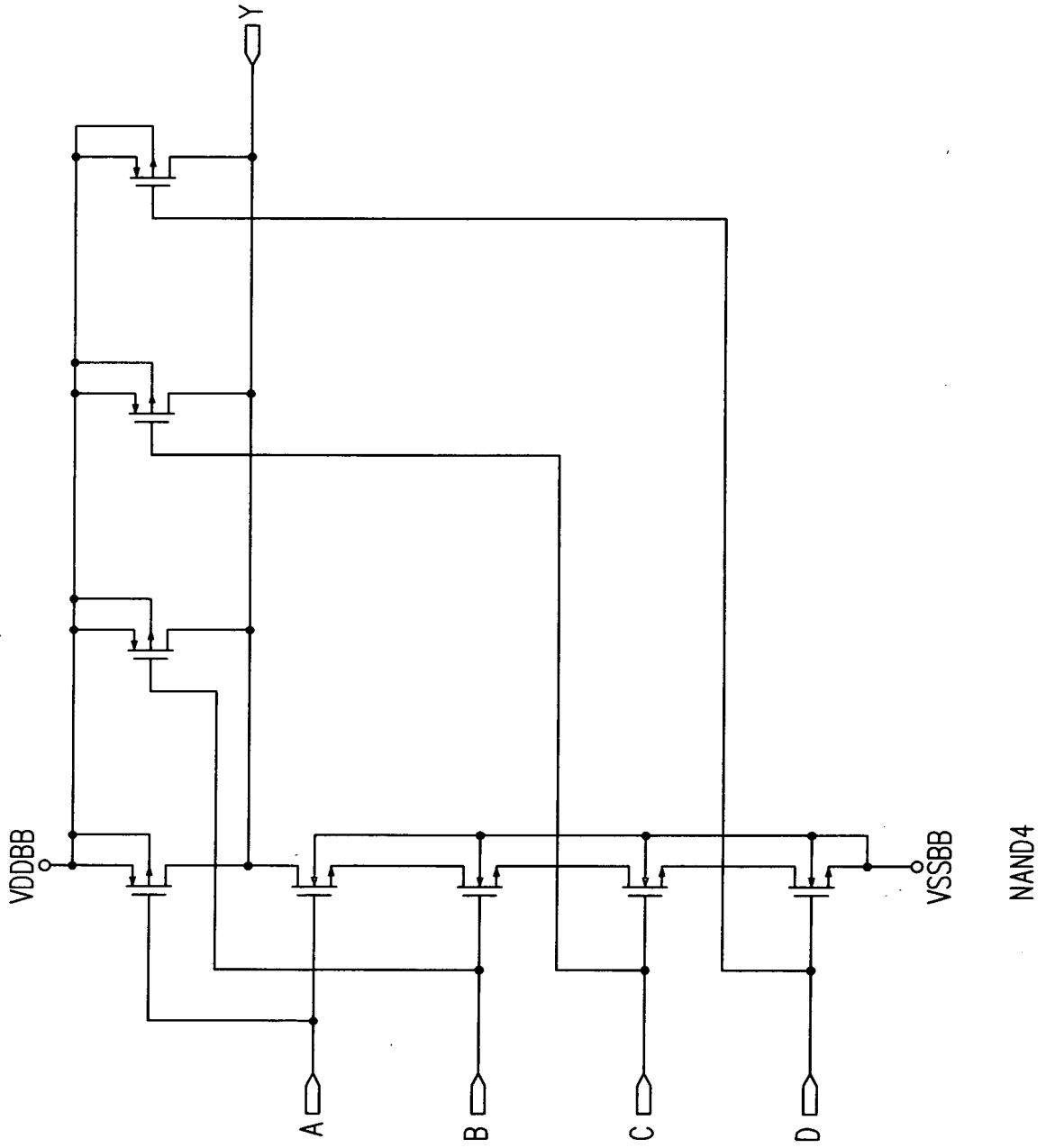


FIG. 73

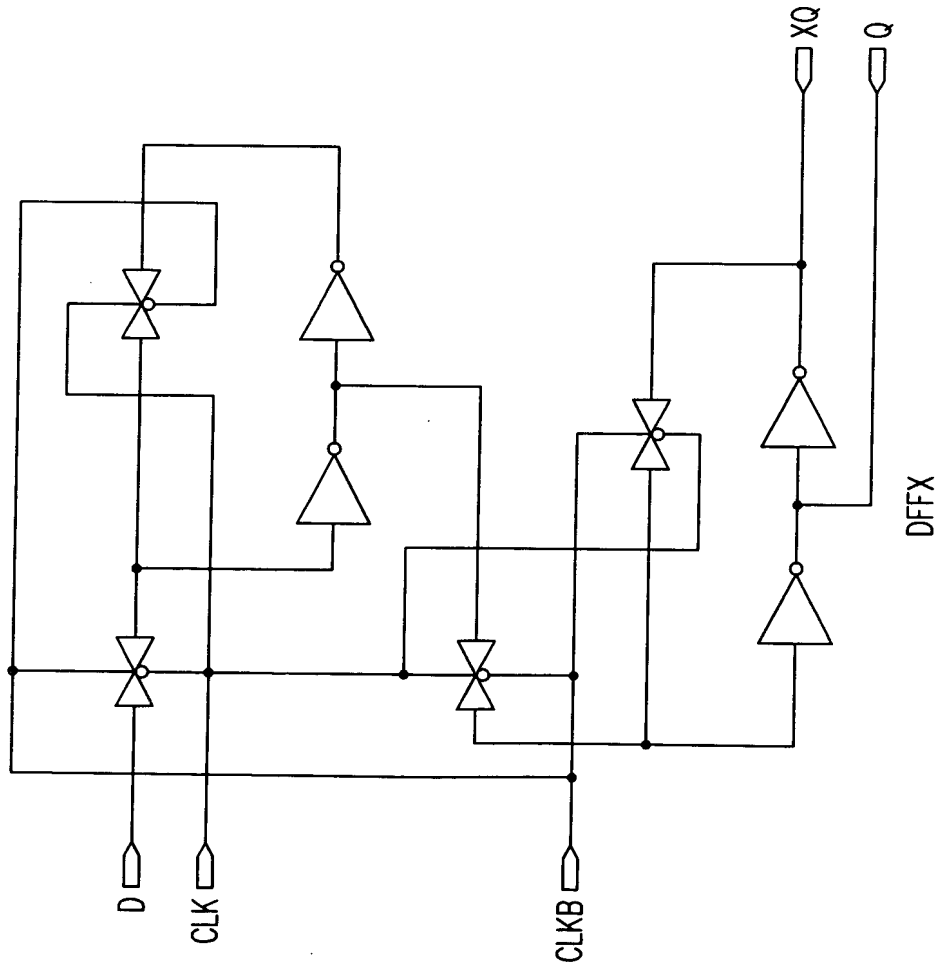
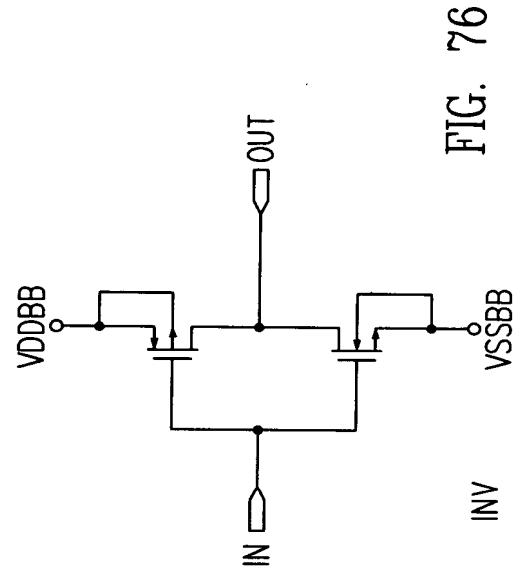
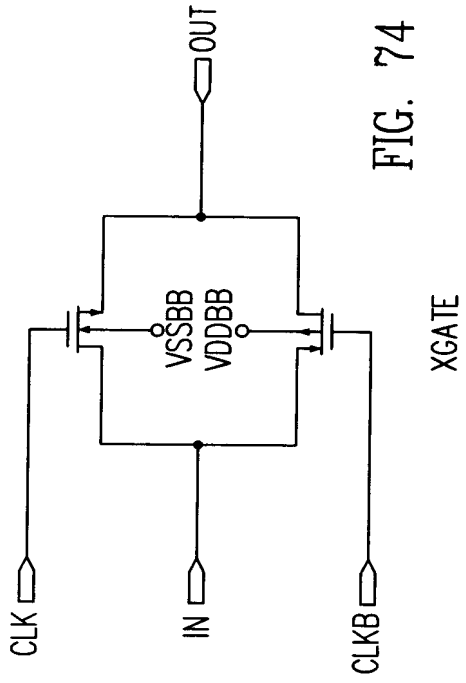


FIG. 75

FIG. 76

FIG. 74